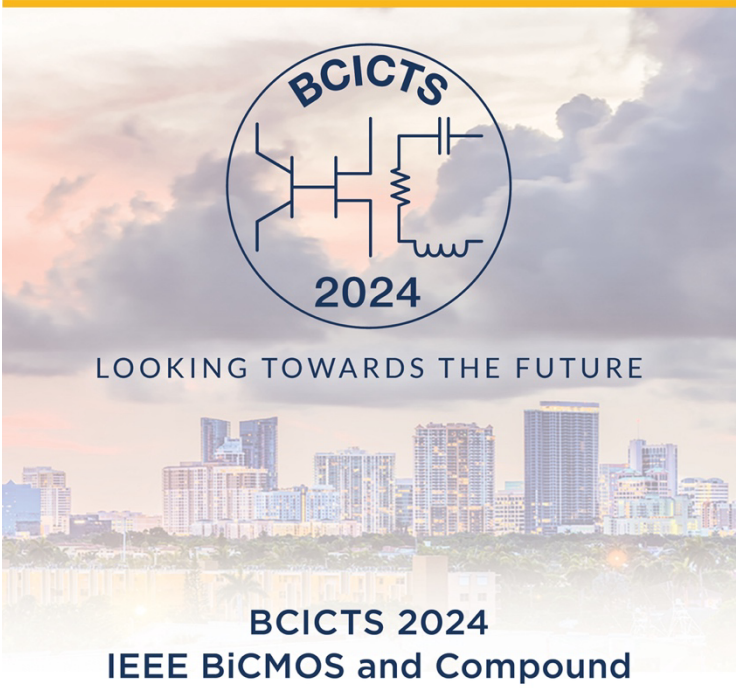
CONFERENCE PROGRAM



BCICTS 2024
IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium

October 27-30, 2024
Ft Lauderdale, FL USA

Sponsored by
The Electron Devices Society of The Institute of Electrical and Electronic Engineers

In Cooperation with
The IEEE Solid - State Circuits Society The IEEE Microwave Theory & Techniques Society

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CONFERENCE WEBSITE
www.bcicts.org

WELCOME FROM THE BCICTS 2024 CHAIRS

With great pleasure we welcome you to participate in the 2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS). After 42 years of the Compound Semiconductor IC Symposium (CSICS), and 35 years of the Bipolar/BiCMOS Circuit and Technology Meeting (BCTM), the seventh meeting of this combined symposium will be held in person from Sunday October 27th to Wednesday October 30th at the W Fort Lauderdale, Florida, USA.

The planning committee looks forward with great anticipation at this opportunity to meet in person again, just like the last two years, after holding two BCICTS conferences virtually due to the COVID-19 pandemic. This a great opportunity for us in the engineering and technical community to reconnect with each other both professionally and personally, to meet new colleagues and visit with long-time friends, while catching up on the latest trends within microelectronics.

This year, BCICTS will continue the long history, from BCTM and CSICS, of international symposiums where distinguished experts present their latest results in bipolar, Si/SiGe BiCMOS, and compound semiconductor circuits, devices, and technology. There are no other events in the world where you can see leading edge bipolar/BiCMOS devices and technology, 5G/6G ICs, GaN HPAs, InP THz PAs, optical CMOS/SiGe transceivers, GaN HEMT power devices, advances in modeling and simulations and device physics, all presented together.

This seventh BCICTS includes presentations from worldwide submissions on all aspects of the technologies. Topics span process technology, device advances, TCAD modeling, compact modeling to IC design and testing, high-volume manufacturing, and system applications. BCICTS will also feature the very latest results in RF/microwave, millimeter-wave, THz, analog & mixed signal, and optoelectronic integrated circuits.

This year, as we have done in past years, BCICTS will offer a topical short course and a more basic primer course. Both will be taught by leading experts, with the short course intended for professionals seeking comprehensive understanding of the latest industry trends and techniques, and the primer as an introductory tutorial.

We would like to thank the many dedicated volunteers on the BCICTS Committee, and the generous support of the IEEE Electron Devices, Microwave Theory and Techniques, and Solid- State Circuits Societies. Finally, we look forward to interacting with all participants to continue the traditions of technical excellence for BCICTS!

Tomislav Suligoj, Symposium Chair
University of Zagreb

Breandán Ó hAnnaidh, Symposium Co-Chair
Analog Devices

KEY EVENT INFORMATION

Meeting Locations:
*Registration is required for attendance

- **Sunday:** Short course, Studio 2&3
- **Sunday:** Primer, Studio#4
- **Monday - Wednesday:**
- **General Session:** Ballroom
- **Breakout:** Studio 2,3,4
- **Exhibition:** Main Foyer
- **Attendee Lounge & Speaker Ready Room:** Studio 1

Conference Networking & Social Events:
Several networking events have been arranged to promote informal social interactions among conference participants. Event details are listed below for your reference:

Monday, October 28: **Exhibitor Reception**
from 5:30 PM - 7:30 PM
Location: Ballroom

Tuesday, October 29:

- **Exhibitor Breakfast:** 7:30 AM - 8:30 AM
- **Exhibitor Luncheon:** 12:30 PM - 2:00 PM

Location: Ballroom Foyer

Registration Desk Hours:
Sunday - Tuesday: 7:30 AM - 5:00 PM
Wednesday: 7:30 AM - 4:00 PM

We're looking forward to seeing you in Fort Lauderdale, Florida!

If you have any questions, please feel free to contact Catherine Shaw:

Catherine Shaw, CMP
Executive Director, Meetings and Events (BCICTS)
Phone: 732-501-3334
E-mail: cs@cshawevents.com

2024 BCICTS SCHEDULE AT A GLANCE

SUNDAY – OCTOBER 27	
SHORT COURSE How to Grow and Model High Reliability III-V Semiconductor Devices **Studio 2&3**	
7:30AM 5:00PM	Registration for Short Course Only **Foyer**
8:00AM 8:45AM	Breakfast for Short Course Only **Foyer**
8:45AM 8:50AM	Welcome & Speaker Introduction, Doug Weiser, Texas Instruments **Studio 2&3**
8:50AM 10:20AM	Epi Growth Dr. Edwin L. Piner Texas State University **Studio 2&3**
10:20AM 10:35AM	Coffee Break for Short Course Only **Ballroom Foyer**
10:35AM 12:05PM	Process/Reliability - Dr. Jose Jimenez Qorvo **Studio 2&3**
12:05PM 1:15PM	Lunch Break for Short Course Only **Studio 5**
1:15PM 2:45PM	Device and Compact Modeling of InP HBTs Dr. Markus Müller TU Dresden, Rohde & Schwarz **Studio 2&3**
2:45PM 3:00PM	Coffee Break for Short Course Only **Ballroom Foyer**
3:00PM 4:30PM	Compact Modeling of GaN HEMTs Dr. Lan Wei University of Waterloo ***Studio 2&3***
4:30PM 4:45PM	Adjourn and feedback
PRIMER Design methodologies for handheld PAs ***Studio 4***	
7:30AM 12:50PM	Registration for Primer Only **Ballroom Foyer**
8:00AM 8:45AM	Breakfast for Primer Only **Ballroom Foyer**
8:45AM 8:50AM	Welcome & Speaker Introduction, M Schroter, TU Dresden ***Studio 4***
8:50AM 11:00AM	Primer Lecture - Part 1, Calogero Presti, Kyocera ***Studio 4***
11:00AM 11:10AM	Coffee Break for Primer Only **Ballroom Foyer**
11:10AM 12:40PM	Primer Lecture - Part 2, Calogero Presti, Kyocera ***Studio 4***
12:40PM 12:50PM	Adjourn and feedback

2024 BCICTS SCHEDULE AT A GLANCE

MONDAY – OCTOBER 28		
7:30AM 5:00PM	Registration/Continental Breakfast **Foyer**	
8:30AM 9:00AM	Welcome and Announcements **Ballroom**	
9:00AM 9:40AM	Plenary Session 1 **Ballroom**	
9:40AM 10:20AM	Plenary Session 2 **Ballroom**	
10:20AM 10:50AM	Sponsored Coffee Break – **Qorvo** **BALLROOM FOYER**	
10:40AM 12:20PM	1a. Advances in Physics-Based HEMT Modeling **Ballroom**	1b. mmW Mixers and Downconverters **Studio 2,3,4**
12:20PM 1:50PM	Lunch Break **Self-Arrangement**	
1:50PM 3:30PM	2a. Applications of III-V Device Modeling **Ballroom**	2b. mmW & THz Transceiver Technology **Studio 2,3,4**
3:30PM 4:00PM	Sponsored Coffee Break – **Texas Instrument** **Ballroom Foyer**	
4:00PM 5:20PM	3a. High Voltage, high performance WBG devices **Ballroom**	3b. Ku-Band and Satellite Circuits **Studio 2,3,4**
5:30PM 7:30PM	Exhibition Reception **Ballroom Foyer**	

TUESDAY – OCTOBER 29		
7:30AM 5:00PM	Registration **Foyer**	
7:30AM 8:30AM	Exhibition Breakfast **Ballroom Foyer**	
8:30AM 2:30PM	Exhibition **Ballroom Foyer**	
8:30AM 10:30AM	4a1. SiGe Technology and Modeling **Ballroom** 4a2. RF Reliability and TCAD to Circuits **Ballroom**	4b. High-Performance Circuits for Optical Communications **Studio 2,3,4**
10:30AM 10:50AM	Coffee Break **Ballroom Foyer**	
10:50AM 12:10AM	5a. Advanced Alloys and Architectures for GaN HEMTs **Ballroom**	5b. Low Noise Amplifiers for mmW Applications **Studio 2,3,4**
12:10PM 1:40PM	Exhibition Lunch **Ballroom Foyer**	
1:40PM 3:20PM	6a. Advanced SiGe Process Technology **Ballroom**	6b. Novel mmW Devices & Design Techniques **Studio 2,3,4**
3:20PM 3:40PM	Coffee Break **Ballroom Foyer**	
3:40PM 5:20PM	7a. III-V Power Amplifiers **Ballroom**	7b. Analog ICs **Studio 2,3,4**

2024 BCICTS SCHEDULE AT A GLANCE

WEDNESDAY – OCTOBER 30		
7:30AM 3:30PM	Registration/Continental Breakfast **Foyer**	
8:30AM 10:10AM	8a. Reliability and physics of Si/SiGe bipolars **Ballroom**	8b. mmW Metrology & Power Amplifier Technology **Studio 2,3,4**
10:10AM 10:30AM	Sponsored Coffee Break – Global Foundries **Ballroom Foyer**	
10:30AM 11:30AM	9a. Diamond and Novel III-V Designs for High Power **Ballroom**	9b. Receiver Circuits **Studio 2,3,4**
11:30AM 1:00PM	Lunch **Self-Arrangement**	
1:00PM 2:40PM	10. Late News **Ballroom**	
2:40PM 3:10PM	Closing Session **Ballroom**	
3:10PM 4:00PM	Reception **Ballroom Foyer**	

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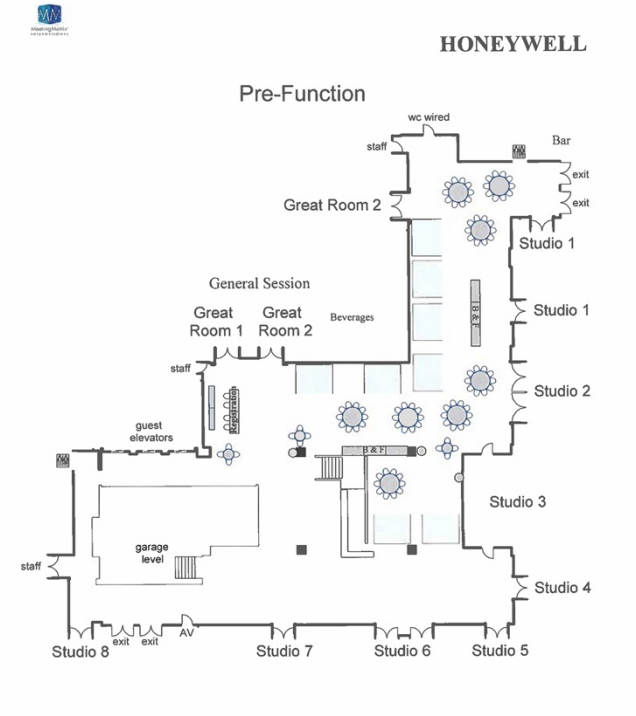

ADDITIONAL INFORMATION

REGISTRATION Complete registration information is contained in the centerfold of this booklet as well as on the conference's web page (https://bcicts.org) Please use the website to register. The advanced registration deadline is **September 13**. All conference activities are included in the registration fees (technical sessions, coffee breaks, Monday exhibition reception, Tuesday exhibition breakfast and Wednesday lunch

CONFERENCE SOCIAL EVENTS Several events have been arranged to promote informal social interactions among conference participants.

TUTORIAL / SURVEY TALKS Tutorial talks given by invited experts are intended to give a broad overview of a given subject with a critical review of technology and applications. They are twice the length of the usual contributed talk with longer abstracts in the Proceedings.

MEMBERS OF THE PRESS: You are welcome to attend BCICTS. Admission is free. Please email Catherine Shaw, CMP, Executive Conference Director at: cs@cshawevents.com for pre-registration and approval by our Executive Committee.

RECRUITING: intensive recruiting undermines the purposes for which the BCICTS was established and is contrary to IEEE policy.

BEST STUDENT PAPER AND BEST PAPER AWARDS
BCICTS offers a Best Paper Award. The BCICTS Best Paper Award recognizes and promotes high quality contributions to scholarly research among professionals who author and present papers at the conference. All papers submitted in non-student category are eligible for consideration for the Best Paper Award.

The BCICTS Best Student Paper Award recognizes and promotes outstanding research led by students. The Best Student Paper Award the following criteria: 1) the student must have carried out a substantial part of the research reported in the paper, 2) the student must be the first author and must present the paper at the conference, 3) the paper must be identified as a student paper during submission of the paper.

Eligible papers have been evaluated by the Best Paper Award Committee and the notifications will be sent out after the conference.

OUR SPONSORS
BCICTS is sponsored by the IEEE Electron Devices Society (EDS) in co - operation with the IEEE Solid - State Circuits Society (SSCS) and the IEEE Microwave Theory & Techniques Society (MTT).

MEETINGS & SESSIONS SCHEDULE DETAILS

SUNDAY

BCICTS 2024 SHORT COURSE

Studio 2&3

- Dr. Edwin L. Piner (Texas State University)
- Dr. Jose Jimenez (Qorvo)
- Dr. Markus Müller (TU Dresden, Rohde & Schwarz)
- Dr. Lan Wei (University of Waterloo)

8:00– 8:45 AM Breakfast (Primer/Short Course Only)

8:45 – 8:50 AM - Welcome & Speaker Introduction
Doug Weiser, Texas Instruments

8:50 – 10:20 AM – III-V Epitaxial & Thin Film Deposition, Processes and Opportunities
Instructor: Dr. Edwin L. Piner, Texas State University

Abstract: Epitaxial and thin film formation processes on single-crystal semiconductor substrates directly enable the various elaborate III-V heterojunction device designs and, therefore, dictate the resulting electronic or optoelectronic device performance. The III-V heterojunction comprises not only the concept of varying dopant species across the junction, but more importantly, also varying the semiconductor crystals and thereby differentiates III-V device design options and concomitant performance benefits over silicon-based devices. The earliest commercially viable example is the AlGaAs/GaAs junction which exploits the energy bandgap difference to engineer charge carrier confinement. GaAs has a narrower bandgap than AlGaAs, and the AlGaAs bandgap may be 'tuned' by precisely controlling the Al composition. Several decades of research have led to the development of III-V heterojunction compounds across the entire semiconductor spectrum; B-, Al-, Ga- and In- from column-III, with N-, P-, As-, and Sb- from column-V of the periodic table. This presentation will delve into the topics of III-V epitaxy and thin film deposition techniques, key process considerations, heterojunction challenges and limitations, and offer perspectives on future opportunities.

Edwin L. Piner received his Ph.D. in Material Science and Engineering from North Carolina State University in 1998. He held multiple research & development related positions in industry beginning with ATMI Corp., Epitronics division in Phoenix, AZ, then with Nitronex Corp. in Durham, NC. In 2010 he joined Texas State University's Physics department, coinciding with the launch of the Materials Science, Engineering & Commercialization Ph.D. program where he attained tenure and promotion to Professor in 2013. In addition to his Texas State faculty appointment, Dr. Piner is Chair of the Physics Department. Dr. Piner has numerous publications in the areas of wide- and ultra-wide bandgap materials and devices, is inventor on 33 US patents, and is a member of MRS, ECS and senior member of IEEE.

10:20 – 10:35 AM Break

10:35 – 12:05 PM GaN Process and Reliability

Instructor: Dr. Jose Jimenez, Qorvo

Abstract: This short course will cover two important aspects of GaN RF Transistor Technology: Device Fabrication and Reliability. On the fabrication section, we will start describing a standard GaN FET process flow, highlighting the differences with its cousin the standard GaAs FET flow. We will cover modules such as ohmics, gate formation, semiconductor passivation, passives and Vias and discuss alternatives within each module. Once the process modules are introduced, we will discuss their main challenges not from the process perspective, but on how they affect the device performance. We will wrap up this section, discussing the challenges and opportunities of improvements as GaN technology moves to nodes designed to cover a higher frequency space or with higher linearity requirements. If time permits, we will cover additional process challenges on alternative sister GaN technologies such as GaN nPolar, GaN Fins, etc …. On the reliability section, we will cover the history behind the intrinsic GaN reliability failure modes, starting with the inverse piezoelectric effect and ending with the chemical reactions responsible for the formation of pitting. In this section, we will also discuss other non-GaN intrinsic failure modes. Though not intrinsic to the GaN material, they have limited the reliability span of the GaN technology. Finally, if time permits, we will attack the challenges of assessing GaN reliability. Though this could seem off topic, it is an essential part of establishing GaN reliability, given the large self-heating and fields the devices are subjected to during operation.

Jose Jimenez is a Sr. R&D Fellow at Qorvo. He received the B.A (1992) in Electrical Engineering from the Universidad Politecnica de Madrid and the Ph. D. (1996) in Electrical Engineering from Columbia University in New York. He is also a La Caixa Fellow and a Beckman Fellow. Jose Jimenez started his professional career working in integrated optics and optoelectronics in Telefonica R&D (Spain), T. J. Watson IBM Research Laboratory, Beckman Institute and Nanovation Technologies. For the last 23 years, he has been part of the R&D organization of TriQuint Semiconductor (Qorvo now) originally leading the efforts first in 4" inch optoelectronics devices (DFB lasers and high speed photo-detectors) and later in GaN FETs. He holds 15 patents and has written more than 100 articles. He is currently a technical committee emeritus chair for the RF/5G/mmW chapter of the International Reliability Physics Symposium, and a committee member of the European Symposium on Reliability of Electron Devices and the Microwave Theory & Technique Society. At Qorvo, Jose is a member of the GaN technology steering and patent Committees.

12:05 – 1:15 PM Lunch

1:15 – 2:45 PM
Device and Compact Modeling of InP HBTs
Instructor: Dr. Markus Müller, TU Dresden, Rohde & Schwarz

Abstract: High-speed Heterojunction Bipolar Transistors (HBTs) based on III-V semiconductors are highly favorable for mm-wave and sub-mm-wave applications due to their high transconductance, transit frequency (f_T), and maximum oscillation frequency (fmax). The most advanced technologies achieve ultra-high f_T > 500 GHz and fmax > 1 THz, but compact and TCAD modeling for these technologies lag behind those for SiGe, necessitating further research. This lecture begins with a review of the most advanced high-speed InP HBTs and their experimental characterization. It will then compare competing III-V HBT technologies based on the InP/GaAsSb and InP/InGaAs material systems. Following this, a review of available compact models and critical effects will be provided, highlighting phenomena such as self-heating, non-quasi-static (NQS) effects, and negative differential mobility (NDM) effects. A high-level overview of the parameter extraction process will be given. Subsequently, the necessary physics and material parameters for TCAD simulation of III-V HBTs will be detailed, along with exemplary results. The session will conclude by highlighting open questions in the field.

Markus Müller earned his Master's in Electrical Engineering in 2019, followed by a Ph.D. in 2024, both from TU Dresden. In 2024, he joined Rohde & Schwarz as a device engineer in the MMIC group. His work focuses on III-V semiconductor compact and TCAD modeling, with several publications in high-impact journals. Additionally, Markus co-founded SemiMod GmbH, where he contributed to the extraction of scalable HICUM/L2 libraries for some of the world's most advanced SiGe HBT technologies.

2:45 – 3:00 PM – Coffee Break

3:00 – 4:30 PM – Compact Modeling of GaN HEMTs
Instructor: Dr. Lan Wei, University of Waterloo

Abstract: With the maturing and commercial rollout of Gallium-nitride (GaN) technology, compact modeling has become an essential part of the GaN design and manufacturing ecosystem. In this short course, we start with a brief introduction of the GaN HEMT technology and the needs of compact modeling, and then discuss the general requirements for compact model and challenges for GaN modeling. A few different approaches of compact modeling will also be compared, followed by a brief introduction of the physics-based MVSG GaN HEMT compact model.

Lan Wei received her B.S. in Microelectronics from Peking University, China (2001), M.S and Ph. D. in Electrical Engineering from Stanford University, USA (2007 and 2010, respectively). She worked as a Postdoc Associate in MIT from 2010-2012 and as a Member of Technical Staff with Altera Corporation from 2012-2014. She joined University of Waterloo, Canada, in 2014, where she is currently an Associate Professor. Prof. Wei has intensive experience in device physics-based compact modeling including silicon and GaN technologies, device-circuit interactive design and

optimization, integrated nanoelectronic systems with low-dimensional materials, cryogenic CMOS device modeling and circuit design for quantum computing. She was listed as one of the key contributors to the Process Integration, Devices, and Structures Chapter (PIDS) of International Technology Roadmap for Semiconductors (ITRS) 2009 Edition. She is the co-developer of the MIT Virtual Source GaN HEMT (MVSG) Compact Model, which is an Industry Standard approved and supported by the Compact Model Coalition for GaN HEMT compact model. She has authored/co-authored more than 100 peered reviewed publications and served on the technical program committees including IEDM, ICCAD, DATE, ISQED, and BCICTS etc.

4:30 – 4:45 PM Adjourn and Feedback

BCICTS 2024 PRIMER

Studio 4

Date: Sunday, October 27, 2024
Time: 8:00 AM – 12:50 PM
Topic: Design methodologies for handheld PAs
Instructor*:* Calogero Presti, Senior Principal Engineer, RFIC Design at Kyocera — Lecturer at UCSD (Power Amps.)

8:00 – 8:45 AM	**Breakfast**
8:45 – 8:50 AM	**Welcome -** *Michael Schröter*
8:50 – 11:00 AM	**Primer Lecture – P1** - *Calogero Presti*
11:00 – 11:10 AM	**Coffee Break**
11:10 – 12:40 PM	**Primer Lecture – P2** - *Calogero Presti*
12:40 – 12:50 PM	**Adjourn and Feedback**

The primer course is an introductory-level course on a selected topic relevant to BCICTS attendees.

Abstract:
In this course, we will delve into the fascinating world of RF power amplifiers (PAs). These essential components play a crucial role in radio transmitters and communication systems. Whether you're a seasoned engineer or just starting out, this session promises valuable insights into the heart of wireless communication.
We'll begin by reviewing the foundational characteristics of modulated signals. Understanding these properties is essential for designing efficient PAs. Signal fidelity, linearity, and distortion will be explored in the context of PA design. We will then dwell into classic PA Theory. Using an idealized transistor model, we'll develop intuition about critical PA concepts, such as loadline tuning (how to optimize the loadline for maximum power delivery), harmonic termination, strategies to improve efficiency, and the definition of the canonical Amplifier Classes (A, B, AB, C). We'll discuss the pros and cons of each amplifier class and their real-world applications.
Then we will approach Practical PA design. We will discuss Class F and J matching topologies, exploring matching networks and efficiency considerations related to second harmonic termination. Then a sample GaAs HBT PA Design will be developed. We will apply theoretical concepts to design a 2-stage PA using a simplified GaAs HBT model. Finally an overview of advanced efficiency enhancement techniques will be given: Doherty and Envelope Tracking.
Join us for an engaging exploration of RF power amplifiers, where theory meets practical design. By the end of this primer, you'll be well-equipped to tackle real-world challenges in RF PA design and optimization.

Calogero D. Presti received the Ph.D. degree in electronics and automation engineering from the University of Catania, Italy, in 2008, working on CMOS Power Amplifiers and Silicon Photonics. During 2009 he was a postdoctoral researcher at UC San Diego, mainly working on PA digital predistortion and envelope tracking. In 2010 he joined Qualcomm Inc., San Diego, CA, where he was part of the team that started the RF Front-End business in the company. There he designed several CMOS and GaAs PAs, and led some front-end module integration for sub-6GHz cellular applications. In 2019 he joined IDT (now part of Renesas) where he designed all the PAs used in mm-Wave beamformers (cellular, satcom, and radar) and occasionally supported the sub-6GHz businesses. Recently, he joined Kyocera, where he designs mm-wave power amplifiers for 5G infrastructure. Since 2017 he teaches the Power Amplifier design class at UC San Diego.

MONDAY

INTRODUCTORY REMARKS AND PLENARY

WELCOME AND ANNOUNCEMENTS
Monday, 8:30 - 9:00 AM
Ballroom
Tomislav Suligoj, Symposium Chair

PLENARY 1

Monday 9:00 AM – 9:40 AM
Ballroom

Session Chair: Tomislav Suligoj, *University of Zagreb*
Co-chair: Michael Roberg, *Qorvo*

Review of DARPA's T-Music Program
Todd Bauer
DARPA Microsystems Technology Office

PLENARY 2

Monday 9:40 AM – 10:20 AM
Ballroom

Session Chair: Michael Roberg, *Qorvo*
Co-chair: Tomislav Suligoj, *University of Zagreb*

The European Chips Act
Yves Gigase
Chips Joint Undertaking

CONFERENCE PROGRAM

1a. Advances in Physics-Based HEMT Modeling
Monday 10:40 AM ***Ballroom***
Session Chair: Lei Zhang, *NXP Semiconductors*
Co-Chair: Subrata Halder, *Qorvo*

1a.1 (Invited)
10:40-11:20 AM – A Family of Physics-Based Models for Monolithic GaN Integration
Lan Wei1, Ryan Fang1, Yijing Feng1, Johan Alant1, Ujwal Radhakrishna2
1 Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, Canada
2 Kilby Research Labs, Texas Instruments Inc., Santa Clara, United States

1a.2 (student)
11:20-11:40 AM – Physics-Based Compact Model for GaN-Based Non-linear Transmission Line Resistors
Johan Alant1, Ryan Fang1, Yuxuan Zhang2, Pilsoon Choi3, Yijing Feng1, Jessica Chong1, Zev Pogrebin2, Bin Lu2, Ujwal Radhakrishna4, Lan Wei1
1University of Waterloo, Waterloo, Canada
2Finwave Semiconductor, Waltham, United States
3Massachusetts Institute of Technology, Cambridge, United States
4Texas Instruments, Santa Clara, United States

1a.3 (student)
11:40-12:00 PM – A Hybrid Physical ASM-HEMT Model Using a Neural Network-Based Methodology
Rafael Perez Martinez1, Masaya Iwamoto2, Ana M. Banzer Morgado1, Yiao Li2, Roberto Tinti3,
Jianjun Xu2, Chad Gillease2, Steven Cochran2, Bhawani Shankar1, Else-Marie Schmidt2,
Zijian Song3, Natalie Wagner2, Philipp Pahl2, Alexander Petr3, and Srabanti Chowdhury1
1Department of Electrical Engineering, Stanford University, Stanford, CA USA
2Keysight Technologies Inc., Santa Rosa, CA USA
3Keysight Technologies Inc., Calabasas, CA USA

1a.4
12:00-12:20 PM – Large-Signal Modeling of a 50 nm mHEMT Incorporating a Physical Impact-Ionization Model
Yasin Yüce, Sayed Ali Albahrani, Dirk Schwantuschke, Arnulf Leuther
Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany

1b. mmW Mixers and Downconverters
Monday 10:40 AM ***Studio 2.3.4***
Session Chair: Daniel Dong, Samsung Research America
Co-Chair: Wooram Lee, Penn State University

1b.1 (Invited)
10:40-11:20 AM – N-Path Mixers Beyond CMOS
Alyosha Molnar
Cornell University, Ithaca, NY, USA

1b.2
11:20-11:40 AM – W-band GaN Resistive FET I-Q Mixer MMICs with Low Conversion Loss
Daniel Kuzmenko[1], Harris Moyer[1], Jana Georgieva[1], Tai Haw[1], Stephen A. Maas[2]
[1]*HRL Laboratories, LLC, Malibu, CA, USA*
[2]*Nonlinear Technologies, Inc., Long Beach, CA, USA*

1b.3 (student)
11:40-12:00 AM – A D-band SiGe Subharmonic Downconverter with Dynamic Conversion Gain and Fixed Input Compression
Jonathan Tao, James F. Buckwalter
Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA, USA.

1b.4 (student)
12:00-12:20 AM – A Sub-Sampling 35GHz PLL in 45nm PDSOI BiCMOS with 37fs Integrated Jitter and a FoM of -252dB
Christopher Chen, Yan Zhang, Hao-Yu Chien, Jiazhang Song, Jia Zhou, Chao-Jen Tien, Sudhakar Pamarti, Chih-Kong Ken Yang, Mau-Chung Frank Chang
Department of Electrical and Computer Engineering, University of California, Los Angeles, CA, USA

2a. Applications of III-V Device Modeling
Monday 1:50 PM ***Ballroom***
Session Chair: John Robert Jones, *BAE Systems, Inc.*
Co-Chair: Masaya Iwamoto, *Keysight Technologies*

2a.1 (Invited)
1:50-2:30 PM – Practical dimensions of contemporary GaN modeling
Larry Dunleavy, Jiang Liu and Hugo Morales
Modelithics, Inc., USA

2a.2 (student)
2:30-2:50 PM – ASM-GaN Model for Resistive Mixer Applications at D-Band Frequencies
Cristina Maurette-Blasini1, Dirk Schwantuschke2, Sayed Ali Albahrani2, Peter Brückner2,
Konstantin Kuliabin1, Sébastien Chartier2, Rüdiger Quay1
1Institute for Sustainable Systems Engineering (INATECH), University of Freiburg, Germany
2Fraunhofer Institute of Applied-Solid-State Physics (IAF), Germany

2a.3
2:50-3:10 PM – Characterization and Large-Signal Modeling of 4-Pole Backgated InGaAs HEMT
Antony Abel Kunnath, Sayed Ali Albahrani, Dirk Schwantuschke, Arnulf Leuther
Fraunhofer IAF, Freiburg, Germany

2a.4 (student)
3:10-3:30 PM – Small-Signal Model Verification and Analysis of Unmatched Multi-Finger HBT Cells at 220 GHz
Rob D. Jones1,2, Jerome Cheron1,3, Benjamin F. Jamroz1, Ari D. Feldman1, and Peter H. Aaen2
1 National Institute of Standards and Technology (NIST), Boulder, CO 80305
2 Colorado School of Mines, Golden, CO 80401
3 Department of Physics, University of Colorado, Boulder CO 80309

2b. mmW & THz Transceiver Technology
Monday 1:50 PM ***Studio 2.3.4***
Session Chair: Marcus Pan, *Semiconductor Research Corporation*
Co-Chair: Kazuya Yamamoto, *Mitsubishi Electric Corporation*

2b.1 (Invited)
1:50-2:30 PM – 300-GHz-Band InP HBT Power Amplifier and InP-CMOS Hybrid Phased-Array Transmitter
T. Jyo[1], I. Abdo[1], H. Hamada[1], M. Nagatani[1], A. Pander[1], H. Wakita[1], M. Mutoh[1], Y. Shiratori[1], D. Kitayama1, C. D. Gomez[2], C. Wang[2], K. Hatano[2], C. Liu[2], A. A. Fadila[2], J. Pang[2], A. Shirane[2], K. Okada[2], H. Takahashi[1]
[1] NTT Device Technology Labs, NTT Corporation, Kanagawa, Japan
[2]Tokyo Institute of Technology, Tokyo, Japan

2b.2
2:30-2:50 PM – 300-GHz 160-Gb/s InP-HEMT Wireless Front-End with Fully Differential Architecture
H. Hamada[1], I. Abdo[1], T. Tsutsumi[2], H. Takahashi[1]
[1]NTT Device Technology Labs, NTT Corporation, Kanagawa, Japan
[2]Department of Physics and Electronics, Osaka Metropolitan University, Osaka, Japan

2b.3 (student)
2:50-3:10 PM – A Q-band Phased-Array Transmit Beamformer in 45nm CMOS SOI for SATCOM
T. Ren, Y. Chang, B. A. Floyd
North Carolina State University, Raleigh, NC, USA

2b.4
3:10-3:30 PM –Full Antenna in Package Solution for 100GHz 6G infrastructure, in 140nm SiGe BiCMOS Technology
P.H.C. Magnée[1], R. Mandamparambil[1], P. Mattheijssen[1], M. Acar[1], K. Giannakidis[1], X. Yang[1], Z. Chen[1], P. Freidl[1], J.J.T.M. Donkers[1], P.G.M. Sebel[1], I. Brunets[1], J.W. Bergman[1], D. Leenaerts[1], A. Ghannam[2], S. Danielsson[1], G. Bisht[3], M. Lal[3], W.-C. Liao[4], O. Tageman[4]
[1]NXP Semiconductors, Eindhoven, Netherlands
[2]3DiS Technologies SAS, Labège, France
[3]Systems on Silicon Manufacturing Company, Singapore
[4]Ericsson Research, Stockholm, Sweden

3a. High Voltage, high performance WBG devices
Monday 4:00 PM ***Ballroom***
Session Chair: Martin Claus, Infineon
Co-Chair: Vibhor Jain, GlobalFoundries

3a.1 (Invited)
4:00-4:40 PM – SiC High-Voltage Power Devices and High-Temperature ICs
T. Kimoto, M. Kaneko, K. Tachiki, K. Ito, K. Mikami, H. Fujii, A. Inoue, R. Ito, and N. Maeda
Department of Electronic Science and Engineering, Kyoto University

3a.2 (Student)
4:40-5:00 PM – High-Temperature Stability Base Ohmic Contacts for InP/GaAsSb DHBTs
F. Ciabattini, A. M. Arabhavi, S. Hamzeloui, G. Bonomo, M. Ebrahimi, O. Ostinelli and C. R. Bolognesi
Millimeter-Wave Electronics (MWE) Group, ETH-Zürich

3b. Ku-Band and Satellite Circuits
Monday 4:00 PM ***Studio 2.3.4***
Session Chair: Michael Litchfield, *BAE Systems*
Co-Chair: Farooq Amin, *Northrop Grumman*

3b.1 (Invited)
4:00-4:40 PM – III-V Semiconductors in Commercial Communication Satellite Payloads
Jim Sowers
Maxar Space Infrastructure, Sunnyvale, CA, USA

3b.2
4:40-5:00 PM – A Ku-Band SiGe:C Power Amplifier with 24.8 dBm Output Power and 35.6% Peak PAE
Christian Bredendiek[1], Jan Wessel[1], Klaus Aufinger[2], Nils Pohl[1,3]
[1] Fraunhofer FHR, Fraunhofer Institute for High Frequency Physics and Radar Techniques FHR, Wachtberg, Germany
[2] Infineon Technologies AG, Neubiberg, Germany
[3] Institute of Integrated Systems, Ruhr-University Bochum, Germany

3b.3
5:00-5:20 PM – A compact low-loss Ku-Band 90° Hybrid Coupler for Front-End Modules in 45 nm SOI CMOS
Evgenii Fedorov and Vadim Issakov
Institute for CMOS Design, TU Braunschweig, Braunschweig, Germany

TUESDAY

4a1. SiGe Technology and Modeling
Tuesday 8:30 AM ***Ballroom***
Session Chair: Breandán Ó hAnnaidh, Analog Devices
Co-Chair: Michael Schroter, *TU Dresden*

4a1.1 (Invited)
08:30-9:10 AM – SiGe BiCMOS or FET Technologies for Wireless PA Applications
Randy Wolf, Shafi Syed, Abdellatif Bellaouar, Chi Zhang, Vibhor Jain, Rebouh Benelbar, Sujata Ghosh, Vivek Tamarkar.
GlobalFoundries – Essex Junction, VT, USA
GlobalFoundries – Dallas, TX, USA
GlobalFoundries – Malta, NY, USA
GlobalFoundries – Bengaluru, India

4a1.2 (Student)
9:10-9:30 AM – Systematic Extraction of Thermal Network Parameters in Multi-Finger SiGe HBTs
Sovan Barman, Subham Pande, Suresh Balenethiram, Thomas Zimmer, Sebastien Fregonese, and Anjan Chakravorty
Indian Institute of Technology, Madras, Chennai, India
National Institute of Technology Puducherry, Karaikal, India
IMS Laboratory, University of Bordeaux, France

4a2. RF Reliability and TCAD to Circuits
Tuesday 9:30 AM ***Ballroom***
Session Chair: Pete Zampardi, *Qorvo*
Co-Chair: Saurabh Sirohi, GlobalFoundries

4a2.1 (Invited)
9:30-10:10 AM – TCAD for Circuits and Cells: Process Emulation, Parasitics Extraction, Self-Heating
Z. Stanojevic, X. Klemenschits, G. Rzepa, F. Mitterbauer, C. Schleich, F. Schanovsky, O. Baumgartner, and M. Karner.
Global TCAD Solutions GmbH, Vienna, Austria

4a2.2
10:10-10:30 AM – On the Safe Operating Area of InP HBTs
Markus Muller, Sebastien Fregonese, Christoph Weimer, Guangsheng Liang, Xiaodi Jin, Maximilian Froitzheim, Thomas Zimmer, and Michael Schroter.
TU Dresden, Germany
IMS Laboratory, CNRS, University of Bordeaux, France

4b. High-Performance Circuits for Optical Communications

Monday 8:30 AM ***Studio 2.3.4***
Session Chair: Munehiko Nagatani, NTT Corporation
Co-Chair: Sorin Voinigescu, *University of Toronto*

4b.1 (Invited)
8:30-9:10 AM – 800 Gpbs Coherent Optical Sub-Assembly (COSA) based on Coupling Modulator Silicon Ring Resonator
A. Rylyakov
Nokia of America Corporation

4b.2 (Invited)
9:10-9:50 AM – Integrated Photonics in Thin-Film Lithium Niobate
C. Reimer
HyperLight

4b.3 (student)
9:50-10:10 AM – Broadband Linear Drivers for 800G/1.6T Energy Efficient Optical Links
M. Hahmud, Hal-Rubaye*, G. Rebeiz
[1] *University of California San Diego*
**Now at Broadcom, Inc.*

4b.4 (student)
10:10-10:30 AM – A 64Gb/s Si-Photonic Micro-Ring Resonator Transceiver with Co-designed CMOS Driver and TIA for WDM Optical-IO
Qianli Ma[1,3] Sikai Chen[1], Jintao Xue[2,3], Yingjie Ma[1,3], Yuean Gu[3], Chao Cheng[2,3], Yihan Chen[3], Haoran Yin[1,3], Guike Li[1,3], Zhao Zhang[1,3], Nanjian Wu[1,3], Ke Li[4], Lei Wang[4], Ming Li[1,3], Chao Xiang[5], Binhao Wang[2,3], Nan Qi[1,3], Liyuan Liu[1,3]*
[1]Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China,
[2]Xi'an Institute of Optics and Precision Mechanics, Chinese Academy of Sciences, Xi'an, China,
[3]University of Chinese Academy of Sciences, Beijing, China,
[4]Peng Cheng Laboratory, Shenzhen, China,
[5]The University of Hong Kong, Hong Kong, China

5a. Low Noise Amplifiers for mmW Applications

Tuesday 10:50 AM ***Ballroom***
Session Chair: Akshay Visweswaran, Nokia Bell Labs
Co-Chair: Ignacio Ramos, HRL Laboratories, LLC.

5a.1
10:50-11:10 AM – A 200-250 GHz Low-Noise Amplifier in 130-nm InP HBT with 15.5 dB Gain and Record 5.3 dB Noise-Figure at 212 GHz
Amirreza Alizadeh[#1], Kwangwon Park[#2], Saleh Hassanzadehyamchi[$3],
Utku Soylu[#4], Miguel E. Urtega[*5], Mark J.W. Rodwell[#6]
[#]University of California, Santa Barbara, CA, USA
[$]University of California, Davis, CA, USA
**Teledyne Scientific, Thousand Oaks, CA, USA*

5a.2 (student)
11:10-11:30 AM – A 7.7-mW DC-to-62 GHz Ultra-Wideband Low-Noise Amplifier with ±2.1 ps Group Delay Variation and 3.3 dB NF in 0.13-mm SiGe:C BiCMOS
Eren Vardarli[#], Austin Ying-Kuang Chen[$], Michael Schroter[#]
[#]TU Dresden, Germany
[$]University of California, Santa Cruz, USA

5a.3 (student)
11:30-11:50 AM – A Biasing Scheme for the Gain Compression Point Optimization of HBT Cascode D-Band LNAs
Lorenzo Serra, Guglielmo De Filippi, Lorenzo Piotto, Andrea Mazzanti
University of Pavia, Italy

5a.4 (student)
11:50 AM-12:10 PM – A 5.6 dB NF Two-Stage 110 - 125 GHz LNA Gain-Boosted by RC-over-Neutralization for Radar Applications in 28 nm CMOS
V. Lasserre[1], S. Koop-Brinkmann[1], M. Caruso[2], D. Dal Maistro[2], G. Volpato[2], Q. H. Le[3], T. Kämpfe[3], C. Ziegler[1], F. Stapelfeldt[1], V. Issakov[1]
[1]Braunschweig University of Technology, Germany
[2]Infineon Austria, Villach, Austria
[3]Fraunhofer Institute for Photonic Microsystems, Dresden, Germany

5b. Advanced Alloys and Architectures for GaN HEMTs
Tuesday 10:50 AM ***Studio 2.3.4***
Session Chair: Tim Vasen, *Northrop Grumman*
Co-Chair: Ken Kikuchi, *Sumitomo Electric*

5b.1 (Invited)
10:50-11:30 AM – Characterization of ScAlN/GaN Toward Electronic Device Application
T. Maeda[1], Y. Wakamoto[1], and A. Kobayashi[2]
[1]University of Tokyo, Tokyo Japan, [2]Tokyo University of Science, Tokyo, Japan

5b.2
11:30-11:50 AM – Performance Limitations of GaN HEMTs with Quaternary InAlGaN and ScAlGaN Barrier Layers
I. Berdalovic, D. Novakovic, and T. Suligoj
University of Zagreb, Zagreb, Croatia

5b.3
11:50 AM-12:10 PM – Design kit development on a 300mm GaN-on-Si demonstration platform with integrated Si pMOS
S. J. Bader1, A Zubair, A. Latorre-Rey, M. Hansen, S. Sarkar, A. Asif, D. Frolov, K. Narayanan, J. Rangaswamy, P. K. Kaur, S. Kumar, N. Kundu, S. S. Jayaprakash, A. Khobragade, P. Yashwanth, Q. Yu, J. Vasudevan, I. Momson, S. Rami, H. Vora, M. Radosavljevic, P. Koirala, M. Beumer, A. Vyatskikh, P. Nordeen, T. Hoff, N. Desai, and H. W. Then
Intel Corporation, Hillsboro, OR, USA

6a. Advanced SiGe Process Technology
Tuesday 1:40 PM ***Ballroom***
Session Chair: Stan Phillips, *Tower Semiconductor*
Co-Chair: Jack Pekarik, *GlobalFoundries*

6a.1 (Invited)
1:40-2:20 PM – A Versatile 55-nm SiGe BiCMOS Technology for Wired, Wireless, and Satcom Applications
P. Chevalier, F. Cacho, C. Durand, N. Derrier, V. Milon, F. Monsieur, A. Gauthier, H. Audouin, M. Buczko, D. Céli, C. Deglise-Favre, C. Diouf, O. Foissey, M. Hello, N. Guitard, S. Madassamy, S. Ramirez-Ruiz, C. Renard, F. Sonnerat, V. Yon, D. Gloria, G. Waltisperger
STMicroelectronics, Technology & Design Platforms, Crolles, France

6a.2
2:20-2:40 PM – Towards 500GHz f_{MAX} 140nm SiGe BiCMOS Technology for 5G/6G Applications
J.P. John[1], J. Kirchgessner[1], J.J.T.M. Donkers[1], P.H.C. Magnée[1], P.G.M. Sebel[1], R. Werkman[1], G. Anderson[1], I. Brunets[1], P.K. Uttwani[2], Mohamed G. Moinuddin[2], L. Radic[1], I. To[1], T.H. Both[1]
[1]*NXP Semiconductors*
[2]*Systems on Silicon Manufacturing Company*

6a.3 (Student)
2:40-3:00 PM – High-Performance SiGe Heterojunction Phototransistor in a Commercial SiGe BiCMOS Platform for Free-Space Optical Receivers
Mozhgan Hosseinzadeh[1], Milad Frounchi[1], George N. Tzintzarov[1]*, Jeffrey W. Teng[1], and John D. Cressler[1]
[1]*Georgia Institute of Technology*
**Now at The Aerospace Corporation*

6a.4
3:00-3:20 PM – Practical Simulation and Test Strategies for Advanced Heterojunction Bipolar Transistors
Adam W. DiVergilio
GlobalFoundries, Essex Junction

6b. Novel mmW Devices & Design Techniques
Tuesday 1:40 PM ***Studio 2.3.4***
Session Chair: Leonardo Vera, Analog Devices
Co-Chair: Harris Moyer, HRL Laboratories, LLC.

6b.1 (Invited)
1:40-2:20 PM – D-Band meets FinFET: Fully-Integrated Transmitter and Receiver Architectures for 100+Gb/s Links
Steven Callender, Abhishek Agrawal, Amy Whitcombe, Ritesh Bhat, Stefano Pellerano
Intel Labs, Intel Corporation, Hillsboro, OR USA

6b.2 (student)
2:20-2:40 PM – A 132-204 GHz Carrier Storage Frequency Divider with sub-50 Micro-Watt DC Power
Sidharth Thomas, Benyamin Fallahi Motlagh, Aydin Babakhani
University of California, Los Angeles, USA

6b.3
2:40-3:00 PM – A Novel Approach to Zero Ω Transmission Line Analysis and Design at W-Band and Beyond
Israel Tapia, Eren Vardarli, Ciro Esposito and Michael Schröter
Technische Universität Dresden, Germany

6b.4 (student)
3:00-3:20 PM – A 10 Gb/s, 120 GHz Compact and Energy-Efficient Harmonic-OOK (HOOK) Modulator using 90 nm SiGe BiCMOS
Shah Zaib Aslam[1] and Najme Ebrahimi[2]
[1]*Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL, USA*
[2]*Department of Electrical and Computer Engineering, Northeastern University, Boston, MA, USA*

7a. III-V Power Amplifiers
Tuesday 3:40 PM ***Ballroom***
Session Chair: Kazuya Yamamoto, *Mitsubishi Electric Corp.*
Co-Chair: David Wohlert, *Qorvo*

7a.1 (Invited)
3:40-4:20 PM – Load-Modulated Balanced Amplifiers for Next-G Wireless Communications
Pingzhu Gong, Jiachen Guo, and Kenle Chen
Department of Electrical and Computer Engineering, University of Central Florida, USA

7a.2
4:20-4:40 PM – Ka-Band, Reactively Matched Non-Uniform Distributed Power Amplifier MMICs in GaN-on-SiC
Michael Litchfield, Qin Shen-Schultz, and Bernard Schmanski
BAE Systems, Nashua, NH, USA

7a.3 (Invited)
4:40-5:20 PM – Advances in GaN HEMT and GaN Power Amplifier Techniques for Base-Stations
Bernhard Grote, David Yu-Ting Wu, Bruce Green, Raphael Holin, David Burdeaux, Philippe Renaud, Humayun Kabir, and Patrick Hu
NXP Semiconductors, Chandler, Arizona, USA

7b. Analog ICs
Tuesday 3:40 PM ***Studio 2.3.4***
Session Chair: Sri Navaneeth Easwaran, Texas Instruments
Co-Chair: Jack Pekarik, GlobalFoundries

7b.1 (Invited)
3:40-4:20 PM – High-Efficiency High-Conversion-Ratio Power Delivery Circuits for Computing Applications
Hoi Lee[1], Chen Chen[1], Weijie Han[1], Atul Sudha[1], Sri Navaneeth Easwaran[2] Jin Liu[1]
[1] *UT Dallas, Texas.*
[2] *Texas Instruments, Dallas, TX*

7b.2 (student)
4:20-4:40 PM – A Single-Stage 24 Gb/s 8:1 Cryogenic Multiplexer for Josephson Arbitrary Waveform Synthesizer
Yerzhan Kudabay[1], Paul Julius Ritter[2], Vadim Issakov[1]
[1] *Institute for CMOS Design, TU Braunschweig, Braunschweig, Germany*
[2] *Institute for Electrical Measurement Science and Fundamental Electrical Engineering, Technical University Braunschweig, Braunschweig, Germany*

7b.3 (student)
4:40-5:00 PM – A Direct Digital Synthesizer-based Arbitrary Waveform Generator for Envelope Modulation in Trapped-Ion Quantum Computer Operating at 4K
Paul Shine Eugine[1], Peter Toth[1], Kaoru Yamashita[2], Sebastian Halama[3], Christian Ospelkaus[3], Hiroki Ishikuro[2], Vadim Issakov[1]
[1] *Institute for CMOS Design, TU Braunschweig, Braunschweig, Germany*
[2] *Ishikuro Laboratory, Keio University, Yokohama, Japan*
[3] *Institute of Quantum Optics, Leibniz University, Hannover, Germany*

7b.4 (student)
5:00-5:20 PM – A Low-Power, High-Swing LDMOS Driver Amplifier for Shuttling Controller in a Trapped-Ion Quantum Computer Operating at 4K
Zhaoqun Guo[1], Alexander Meyer[1], Adilet Dossanov[1], Paul Julius Ritter[2], Marius Neumann[2], Jens Repp[3], Matthias Brandl[3], Meinhard Schilling[2], Vadim Issakov[1]
[1] *Institute for CMOS Design, TU Braunschweig, Braunschweig, Germany*
[2] *Institute for Electrical Measurement Science and Fundamental Electrical Engineering, TU Braunschweig, Braunschweig, Germany*
[3] *Infineon Technologies AG, Neubiberg, Germany*

WEDNESDAY

8a. Reliability and physics of Si/SiGe bipolars
Wednesday 8:30AM ***Ballroom***
Session Chair: Kai Kwok, Skyworks
Co-Chair: Jonggook Kim, Texas Instruments

8a.1
8:30-8:50 AM – High Temperature Annealing induced recovery of Hot-Carrier degradation in High Performance NPN SiGe HBTs
Dimitris P. Ioannou and Adam DiVergilio
GlobalFoundries, USA

8a.2 (Student)
8:50-9:10 AM – Using Pulsed-Mode Measurements of SiGe HBTs for Non-Destructive, Improved RF-SOA Estimation
Nelson E. Sepúlveda-Ramos, Harrison P. Lee, Jeffrey W. Teng, and John D. Cressler
School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA

8a.3 (Student)
9:10-9:30 AM – The Effect of Base Doping Profile on Horizontal Current Bipolar Transistor's (HCBT) Beta Recovery at Cryogenic Temperatures
Filip Bogdanović[1], Lovro Marković[1], Azra Tabaković[1], Josip Žilak[2], Marko Koričić[1] and Tomislav Suligoj[1]
[1]University of Zagreb, Faculty of Electrical Engineering and Computing, Micro and Nano Electronics Laboratory, Zagreb, Croatia
[2]Ericsson Nikola Tesla d.d., Zagreb, Croatia

8a.4
9:30-9:50 AM – On the Emitter Back-Injection Current in Advanced SiGe HBTs at Cryogenic Temperatures
Xiaodi Jin, Prateek Kumar, and Michael Schröter
Chair for Electron Devices and Integrated Circuits, Technische Universität Dresden, Germany

8a.5 (Student)
9:50-10:10 AM – TCAD-Based Design of SiGe HBT Germanium Profiles via Bayesian Optimization
Justin P. Heimerl, Jeffrey W. Teng, Harrison P. Lee, Delgermaa Nergui, Jackson P. Moody, and John D. Cressler
School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA

8b. mmW Metrology & Power Amplifier Technology
Wednesday 8:30AM ***Studio 2.3.4***
Session Chair: Harris Moyer, HRL Laboratories, LLC.
Co-Chair: Utku Soylu, IBM T.J. Watson Research Center

8b.1 (Invited)
8:30-9:10 AM – Trends in Millimeter-Wave and THz Test Equipment
Eric Bryerton, Jeffrey Hesler
Virginia Diodes, Inc., Charlottesville, VA, USA

8b.2 (student)
9:10-9:30 AM – A D-band Power-Combined Stacked Common-Base Power Amplifier Achieving 20.9 dBm Psat and 24.3 % PAE in a 250-nm InP HBT Technology
Arno Hemelhof[*†], Sehoon Park[‡], Yang Zhang[*], Mark Ingels[*], Giuseppe Gramegna[*], Kristof Vaesen[*], Dongyang Yan[*†], Piet Wambacq[*†]
[*]*imec, Leuven, Belgium*
[†]*Vrije Universiteit Brussel, Dept. of Electronics and Informatics (ETRO), Brussels, Belgium*
[‡]*now with Kyungpook National University, School of Electronics Engineering, Daegu, Republic of Korea*

8b.3 (student)
9:30-9:50 AM – A Two-stage, Two-way-combined, 220-GHz Power Amplifier With 17.1% PAE in a 250-nm InP HBT Process
Eythan Lam[#], Jeff Shieh-Chieh Chien[#$], Petra Rowell*, Miguel Urteaga*, James Buckwalter[#]
[#]*University of California, Santa Barbara, USA*
[$]*Samsung Semiconductor, Inc., San Jose, USA*
**Teledyne Scientific and Imaging, Thousand Oaks, USA*

8b.4 (student)
9:50-10:10 AM – 10-GSymbols/s Supply Modulated 250-GHz SiGe HBT Transmitter RF Front-End with 6.8-dBm Peak Modulated Power
Haidong Guo[1], Suprovo Ghosh[1], Frank Zhang[1], Suhwan Lee[1], Wooyeol Choi[2], Shenggang Dong[1], Kenneth O[1]
[1]*University of Texas at Dallas, Richardson, TX, USA*
[2]*Seoul National University, Seoul, Korea*

9a. Diamond and Novel III-V Designs for High Power
Wednesday 10:30 AM ***Ballroom***
Session Chair: Kanin Chu, *BAE Systems*
Co-Chair: Takuya Hoshi, *NTT*

9a.1 (Invited)
10:30-11:10 AM – Diamond-BN Heterojunctions for High Power Devices: The Ultimate HEMT?
T. Thornton
Arizona State University, Tempe, AZ USA

9a.2
11:10-11:30 AM – Exploring Breakdown Voltage Improvement in 20-nm InGaAs-Channel HEMT-OI with Metallic Back-Gate
A. A. Kunnath, M. Moulin, S. A. Albahrani, D. Schwantuschke, and A. Leuther
Fraunhofer IAF, Freiberg, Germany

9b. Receiver Circuits
Wednesday 10:30 AM ***Studio 2.3.4***
Session Chair: Gregory Flewelling, *BAE Systems*
Co-Chair: Django Trombley, *TI*

9b.1
10:30-10:50 AM – A 19.1-dBm-Linear 2-20 GHz N-path Down-converter in HRL 40-nm GaN for Resilient Receivers
Robin Ying and Joe Tai
HRL Laboratories LLC, Malibu, CA, USA

9b.2
10:50-11:10 AM – Single-Chip 30 GHz SiGe Sub-Sampling PLL with 28.3 fs Jitter
Dimitre Dimitrov, Mark D. Hickle, Matthew Speir, Joseph M. Krzyzek, Daniel P. Lacroix, Shail Srinivas, Robert Sepanek, Spencer Desrochers, and Steven Eugene Turner
BAE Systems, Merrimack, NH, USA

9b.3 (Student)
11:10-11:30 AM – Design of an Ultra-Low Phase Noise Broadband Amplifier in 130 nm SiGe BiCMOS Technology
Vijayalakshmi Surendranath Shroff, Meysam Bahmanian, Stephan Kruse, and J. Christoph Scheytt
Paderborn University, Department of Electrical Engineering, Heinz Nixdorf Institute, Germany

10. Late News
Wednesday 1:00 PM ***Ballroom***
Session Chair: Jack Pekarik, GlobalFoundries
Co-Chair: Sadayuki Yoshitomi, MegaChips Corporation

10.1 (student)
1:00-1:20 PM – Design of a Terahertz InP HBT Quadrupler and Silicon Interposer
Vinay Iyer[1,2], Christopher Moore[2], Prerana Singaraju[2], Matthew F. Bauwens[3], Steven M. Bowers[2], Robert M. Weikle[2]
[1]Nokia of America Corporation, Sunnyvale, CA, USA
[2]University of Virginia, Electrical and Computer Engineering, Charlottesville, VA, USA
[3]Dominion Microprobes, Charlottesville, VA, USA

10.2 (student)
1:20-1:40 PM – A 130-GHz Bandwidth 61-dBOhm Variable-Gain Differential Linear TIA in a 130-nm SiGe:C BiCMOS Technology
Thiemo Herbel[1], Mohsin Tarar[2], Frank Vater[3], Dietmar Kissinger[1]
[1]Institute of Electronic Devices and Circuits, Ulm University, Ulm, Germany
[2]Department of Electronics Engineering, University of Chakwal, Chakwal, Pakistan
[3]Leibniz Institute for High Performance Microelectronics (IHP), Frankfurt (Oder), Germany

10.3
1:40-2:00 – 140-GHz Transmit and Receive Front-end Circuits with 10.8-dBm Psat and 5.9-dB NF in a 45-nm BiCMOS SOI Process
Wonho Lee, Everett O'Malley, James Buckwalter
Electrical & Computer Engineering, UC Santa Barbara, Santa Barbara, CA

10.4
2:00-2:20 – The Design of Wideband LNAs in 45nm SiGe BiCMOS
David Dolt[1], Mingi Yeo[1], David Reents[1], Will Gouty[2], Tony Quach[2], Samuel Palermo[1]
[1]Texas A&M University, Analog and Mixed-Signal Center, College Station, TX, USA
[2]Air Force Research Laboratory, Sensors Directorate, WPAFB, OH, USA

10.5 (student)
2:20-2:40 – Ka-Band MMIC Implementation of a Load-Modulating Loop Combiner Power Amplifier
Osian Jones, Taylor Barton
RF Power and Analog Laboratory, University of Colorado Boulder, Boulder, CO, 80309 USA

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Compound Advanced Devices and Technologies

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Ken Chu	BAE Systems
Bruce Green	NXP Semiconductors
Rob Howell	Northrup Grumman Mission Systems
Takuya Hoshi	NTT Device Technology Laboratories
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Martin Claus	Infineon
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Koichi Murata	Renesas
The' Linh Nguyen	Marvell
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Silicon and Related Alloy Semiconductor Processing

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Holger Rucker	IHP Microelectronics
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LOOKING TOWARDS THE FUTURE

The 2025 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) will be held on October 12-15, 2025 Scottsdale, Arizona, USA

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HIGH-SPEED DIGITAL, MIXED-SIGNAL, AND OPTOELECTRONIC ICs Mixed analog/digital ICs - Digital ICs - (high-speed) DACs and ADCs - Networking ICs, MUX/DEMUX, Clock and data recovery, Decision circuits, Equalizers - Optical data links, Laser and modulator drivers, optoelectronics and photonics ICs

ANALOG, RF, AND MICROWAVE ICs
Op amps - Voltage references and regulators - Integrated filters - Sensors and actuators - RF circuits and systems - Radio and transceiver subsystems - LNAs - AGCs - Mixers - Voltage controlled oscillators - Frequency synthesizers - Power amplifiers - RF switches - Noise and distortion suppression - RF Packaging - Integrated RF passives. Analog, RF, power conversion, High-voltage ICs - Biomedical electronics - Power Management ICs - Energy harvesting ICs - Motor controls - Analog subsystems within a VLSI chip - Packaging of high-performance ICs.

mm-WAVE AND THZ ICs
Millimeter - wave circuits and systems - THz circuits and systems. MM-Wave switches and amplifiers. Phased-array antenna circuits

DEVICE PHYSICS:
New device physics phenomena in Si, SiGe, SiC, GaN, MOS, and III-V HBTs and FETs - Device design issues and scaling limits - Hot electron effects and reliability physics - Transport and high field phenomena - Noise - Linearity/Distortion - Novel measurement techniques - Operation in extreme environments (low/high temperatures, radiation effects), and ESD phenomena.

MODELING AND SIMULATION
Improved silicon-based BJT and HBT models and physics-based modelling techniques - Improved III-V HBT and FET models and physics-based modelling techniques - Parameter extraction methods and test structures - High-frequency measurement, calibration and de-embedding techniques - RF and thermal simulation techniques - Modelling of passives, interconnect and packages - Statistical modelling - Device, process and circuit simulation - CAD/modelling of power devices - Packaging of power devices.

PROCESS AND DEVICE TECHNOLOGY
Device and IC manufacturing processes, testing methodologies, & reliability - Integration of III-V devices on Si - High performance devices such as GaN power conversion devices - near-THz SiGe HBTs & InP HEMTs - Novel devices such as tunnel FETs (TFETs) - carbon nanotubes, MEMS, graphene & diamond transistors. Optoelectronic and photonic devices such as optical modulators, lasers, photodetectors, and Silicon Photonics - Thermal management technologies, thermal simulation - Advanced packaging of high-power devices and ICs. Advances in processes and device structures demonstrating high speed, low power, low noise, high current, high voltage, etc. BiCMOS processes - Advanced process techniques - Si and SiC homojunction bipolar/BiCMOS devices and SiGe heterojunction bipolar/BiCMOS devices - Manufacturing solutions related to Bipolar and BiCMOS yield improvements - Fabrication of high-performance passive components, sensors, and MEMs - Process technology related to discrete and integrated bipolar/BiCMOS power devices - IGBT, RF power devices. Wide bandgap bipolar devices (e.g., SiC) and related process technology - 3D Integration - Reliability and testing for IC manufacturing

IMPORTANT DATES
Friday May 9, 2025 – Abstracts Due
Friday, July 11, 2025 – Decision E-mail Sent
Friday, September 5, 2025 – Final Manuscript Due

Authors must submit an abstract (not more than 4 pages including figures and other supporting material) of results not previously published or not already accepted by another conference. Papers will be selected on the basis of the abstract.

The abstract must concisely and clearly state:

a) The purpose of the work
b) What specific new results have been obtained
c) How it advances the state-of-the-art or the industry
d) References to prior state-of-the-art
e) Sub-committee preference:
   - Analog, RF, and Microwave ICs
   - Device Physics
   - High-Speed Digital, Mixed-Signal, & Optoelectronic ICs
   - Modeling & Simulation
   - mm-Wave and THz ICs
   - Process & Device Technology

Abstracts must include: title, author(s) name(s) and affiliation(s), corresponding authors' postal and e-mail addresses, and telephone numbers. The committee will honor the authors' committee preference but reserves the right to review the paper in other categories.

Company and governmental clearances must be obtained prior to submission of the abstract.

Accepted work may be used for publicity purposes. Portions of the abstracts may be quoted in articles publicizing the Symposium. Please note on the abstract if this is not acceptable.

Abstracts (PDF only) must be submitted electronically.

Authors will be informed of a decision by July 11, 2025. Authors of accepted papers are required to submit a 4-page camera-ready PDF by September 5, 2025 for inclusion in the Symposium Digest.

Further questions on abstract submission may be addressed to the Symposium Technical Chair:

Michael Roberg
Technical Director, MMIC Design
Qorvo, Inc.
Email: michael.roberg@qorvo.com

Symposium information, including abstract submission instructions and a link to the abstract submission system will be available on the BCICTS website at: http:// www.bcicts.org in the near future.

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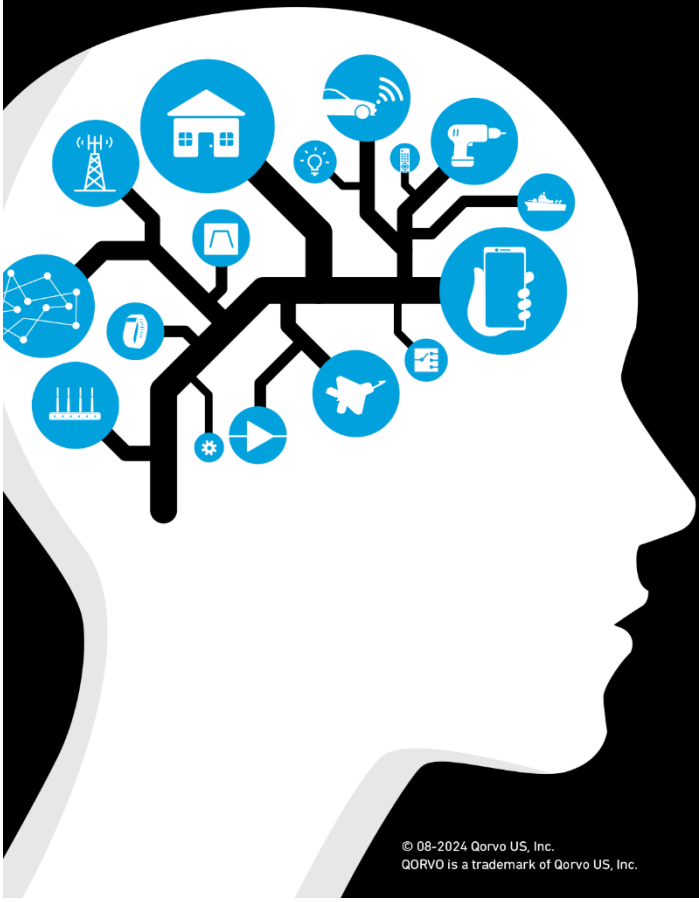


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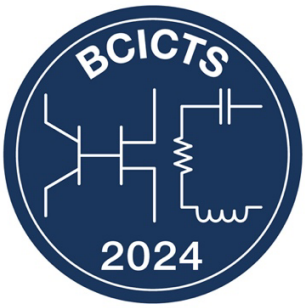

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