ADVANCE PROGRAM

BCICTS 2018
IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium

Sheraton San Diego Hotel and Marina
San Diego, California, USA

October 14 - 17, 2018
SHORT COURSE - October 14, 2018
PRIMER - October 15, 2018

SPONSORED BY

THE ELECTRON DEVICES SOCIETY OF THE INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS

IN COOPERATION WITH

THE IEEE SOLID - STATE CIRCUITS SOCIETY
THE IEEE MICROWAVE THEORY & TECHNIQUES SOCIETY

Conference Website: https://bcicts.org

2018 BCICTS SCHEDULE AT A GLANCE		
Sunday - October 14		
SHORT COURSE ONLY Registration & Breakfast at 7:00 AM **Bel Aire Foyer**		
7:45AM - 4:00PM	**SHORT COURSE** ***Phased Arrays and Massive MIMO: Technology and Systems*** ***Bel Aire Ballroom South*** ***Lunch Bel Aire Ballroom North*** ***(Short Course attendees only)***	
Monday - October 15		
Registration opens at 7:00 AM **Bel Aire Foyer**		
8:00AM - 12:00PM	PRIMER COURSE ***SiGe Technology and mmW Layout Techniques*** ***Bel Aire Ballroom South***	
12:00PM - 1:10PM	**Lunch Break** ***(Self - Arrangement)***	
1:10PM - 1:40PM	Welcome and Announcements **Bell Aire Ballroom**	
1:40PM - 3:40PM	Plenary Session **Bell Aire Ballroom**	
3:40PM - 4:00PM	Coffee Break	
4:00PM - 5:10PM	**1**. Optical Communications **Bell Aire Ballroom North**	**2**. Applications of GaN HEMT Modeling **Bell Aire Ballroom South**
5:40PM - 7:30PM	Exhibition Reception **Fairbanks Ballroom**	
Tuesday - October 16		
Registration opens at 7:00 AM **Bel Aire Foyer**		
7:00AM - 8:00AM	Exhibitor Breakfast **Fairbanks Ballroom**	
8:00AM - 9:10AM	**3.** Data Converter Circuits **Bell Aire Ballroom North**	**4.** State-of-the-Art SiGe BiCMOS **Bell Aire Ballroom South**
9:10AM - 9:30AM	Coffee Break	
9:30AM - 10:40AM	**5.** 5G Components and Systems **Bell Aire Ballroom North**	**6.** Advances in GaN Modeling **Bell Aire Ballroom South**
10:40AM - 11:00AM	Coffee Break	
11:00AM - 12:00PM	**7.** High Frequency Characterization **Bell Aire Ballroom North**	**8.** Extreme Bandwidth mmW Circuits **Bell Aire Ballroom South**
11:30AM - 1:00PM	**Exhibition Lunch** **Fairbanks Ballroom**	
1:10PM - 2:30PM	**9**. Emerging Compound Semiconductor Device Technology **Bell Aire Ballroom North**	**10**. Power Amplifiers and Supporting Circuits **Bell Aire Ballroom South**
2:30PM - 2:50PM	Coffee Break	
2:50PM - 4:20PM	**11**. Sub-Terahertz Amplifiers and Technology **Bell Aire Ballroom North**	**12**. Silicon Based Device Physics and Reliability **Bell Aire Ballroom South**
5:45 PM - 10:00 PM	**BANQUET** **GATHER IN THE BAY TOWER LOBBY AT 5:45 PM**	

Wednesday - October 17 Registration opens at 8:00 AM **Bel Aire Foyer**		
9:00AM - 10:20AM	**13.** Advanced Circuits in SiGe Technology **Bell Aire Ballroom North**	**14.** SiGe Modeling **Bell Aire Ballroom South**
10:20AM - 10:40AM	Coffee Break	
10:40AM - 12:00PM	**15.** mmW Transceivers **Bell Aire Ballroom North**	**16.** GaN Devices and Packaging **Bell Aire Ballroom South**
12:00PM - 1:10PM	**Lunch Break** ***(Self - Arrangement)***	
1:10PM - 2:30PM	**17**. Late News 1 **Bell Aire Ballroom North**	**18**. Late News 2 **Bell Aire Ballroom South**
2:30PM - 2:50PM	Coffee Break	
2:50PM - 3:50PM	**19**. Late News 3 ***Bell Aire Ballroom***	
3:50 PM - 4:10 PM	Coffee Break	
4:10 PM - 5:00 PM	Closing Session	

Welcome from the BCICTS 2018 Chairmen

It is with great pleasure that we welcome you to be a part of the 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS). After 39 years of the Compound Semiconductor IC Symposium (CSICS), and 32 years of the Bipolar/BiCMOS Circuit and Technology Meeting (BCTM), this new combined symposium will be held on Sunday October 14 to Wednesday October 17 in San Diego, Sunny California.

Both BCTM and CSICS bring a long history as international gatherings where distinguished experts present their latest results in bipolar, SiGe BiCMOS, and compound semiconductor circuits, devices, and technology. There are no other events in the world where you can see leading edge bipolar/BiCMOS devices and technology, 5G ICs, GaN HPAs, InP THz PAs, optical CMOS/SiGe transceivers, GaN HEMT power devices, and advances in compact modeling all presented together.

This first BCICTS includes presentations from worldwide submissions on all aspects of the technology. Topics span process technology, device advances, TCAD modeling, compact modeling to IC design and testing, high-volume manufacturing, and system applications. BCICTS will also feature the very latest results in RF/microwave, millimeter-wave, THz, analog mixed signal, and optoelectronic integrated circuits.

On Sunday October 14th, BCICTS offers a topical short course “Phased Arrays and Massive MIMO: Technology and Systems”. On Monday morning October 15th, BCICTS offers a primer course: “SiGe Technology and mmW Layout Techniques”. Taught by leading experts, the short course is intended for both technologists and IC designers who seek a comprehensive understanding of the latest industry trends and techniques. The primer course is intended to be a tutorial which introduces key concepts, techniques and practices for RF circuit design.

As a complement to the technical program, the symposium includes numerous social events that allow participants to interact and network in a friendly, relaxed setting. These events include the Monday Evening Exhibition Opening Reception, and the Technology Exhibition Luncheon on Tuesday. BCICTS will also offer a banquet on Tuesday evening, in nearby Tom Ham’s Lighthouse.

We would like to thank the many dedicated volunteers on the BCTM and CSICS organizing committees, now merged into one BCICTS Committee, and the generous support of the IEEE Electron Devices, Microwave Theory and Techniques, and Solid-State Circuits Societies. Finally, we look forward to interacting with all participants to create a new and exciting symposium tradition!

Peter Magnee
Symposium Co-chair
NXP

Brian Moser
Symposium Co-chair
Qorvo

BCICTS 2018 REGISTRATION

Click here to register https://bcicts.org
Advance registration deadline is Friday, September 7, 2018.

Registration Fees: MAIN MEETING (October 15-17)
Please contact cs@cshawevents.com for more details.

(1) Conference Registration Cost in US Dollars (includes conference program, electronic proceedings, exhibition opening reception, exhibition lunch, banquet, and all day refreshments)

	ADVANCE	REGULAR
	By 9/7/2018	Starting 9/7/2018
IEEE Members	$725	$825
Non-Members	$775	$875
Students	$400	$450

(2) Guest Fee for Dinner Banquet

	$125/person	$135/person

(3) Extra 2018 Proceedings (electronic version on USB drive):

IEEE Members	$50
Non-Members	$75

Registration Fees: SHORT COURSE (October 14)
(1) Course Cost (includes breakfast and lunch)

Regular	$520	$520
Students	$270	$270
Extra USB	$100	

Registration Fees: PRIMER (October 15)
(1) Course Cost (includes breakfast and lunch)

Regular	$370	$370
Students	$220	$220
Extra USB	$100	

Notes:
*All fees are denominated in US$
*Full Registration for the conference Includes: proceedings, all day refreshments, some lunches, vendor reception, and a banquet dinner at Tom Han's Light house.

*Short Course Registration includes: short course notes/USB, continental breakfast, lunch and light refreshments

*Primer course registration includes: primer course notes/USB

Refund/Cancellation Policy:
All requests for refund/cancellation must be received in writing at least 10 days prior to the conference start date for a full refund on or before September 28, 2018. Any requests thereafter will not be entitled to a refund. Cancellations will incur a $50 USD administration fee. Please submit cancellation requests via email (cs@cshawevents).

BEST STUDENT PAPER AND BEST PAPER AWARDS BCICTS offers a Best Paper Award. The BCICTS Best Paper Award recognizes and promotes high quality contributions to scholarly research among professionals who author and present papers at the conference. All papers submitted in non-student category are eligible for consideration for the Best Paper Award.

The BCICTS Best Student Paper Award recognizes and promotes outstanding research led by students. To be eligible for consideration for the Best Student Paper Award, the following criteria have to be met: 1) the student must have carried out a substantial part of the research reported in the paper, 2) the student must be the first author and must present the paper at the conference, 3) the paper must be identified as a student paper during submission of the paper; and 4) the paper identified as a student paper in submission, but not presented by the student will be disqualified for Best Student Paper Award competition. In this scenario, the paper will be moved to non - student category for Best Paper Award competition automatically.

Eligible papers are evaluated by the Best Paper Award Committee and the notifications will be sent out after the conference. The winners of the awards will be recognized with a $500 check and a plaque at next year's BCICTS conference.

FURTHER INFORMATION BCICTS is sponsored by the IEEE Electron Devices Society (EDS) in co - operation with the IEEE Solid - State Circuits Society (SSCS) and the IEEE Microwave Theory & Techniques Society (MTT).

ADMISSION All interested persons are welcome to register and attend the BCICTS; you do not have to be an IEEE member. Admission to sessions requires a BCICTS name badge. Please wear your badge at all times.

REGISTRATION Complete registration information is contained in the conference's web page (https://bcicts.org) Please use the website to register. All conference activities are included in the registration fees (technical sessions, food breaks and the banquet) as well as a USB flash drive with an electronic copy of BCICTS 2018 Proceedings.

TUTORIAL / SURVEY TALKS Tutorial talks given by invited experts are intended to give a broad overview of a given subject with a critical review of technology and applications. They are twice the length of the usual contributed talk with longer abstracts in the Proceedings.

MEMBERS OF THE PRESS: You are welcome to attend BCICTS. Admission is free. Just present your business card at the registration desk.

RECRUITING Intensive recruiting undermines the purposes for which the BCICTS was established, and is contrary to IEEE policy.

HOTEL RESERVATIONS

A block of rooms has been reserved at special discounted rates for BCICTS conference participants at our host hotel below. While there are alternatives, we would like to remind attendees to please support the conference and fully enjoy all the activities by staying at the official host hotel. The symposium relies on attendees staying at the conference hotel. Room reservations should be made as soon as possible before the hotel cut-off date below, as there are a limited number available at the group rate.

Sheraton San Diego Hotel & Marina
1380 Harbor Island Drive
San Diego, CA 92101

Check-in Time: 4:00 pm Check-out Time: 12:00 pm
Group Hotel Rates $239.00 plus tax (12.695%)
Book your room at the group rate by clicking here.

Hotel Accommodations

Room Reservation: You are responsible for booking your hotel room at the host hotel.
Click here to reserve your room or call reservations at 1-877-734-2726. You must reference IEEE or BCICTS or BCICTS 2018 Conference when making your reservation. Room, tax, and incidentals will be billed to the credit card you provide.

Guest Room Rate: Single / Double $239.00 plus tax (12.695%)
Group Rate will be provided 3 days before and after meeting dates (October 14-17, 2018), based on availability.

- Reservation Cut-Off Date: Reservations must be made by the cut-off date, Wednesday, September 19, 2018 by 5:00 PM PST in order to receive the group rate and guarantee availability. After this date, rooms will be on a space available basis and at possibly higher rates. We recommend you book early.
- Changes or Cancellations: Contact the hotel directly.

Internet & Parking

- Internet access is available in all guest rooms. Marriott/SPG Rewards Members will receive complimentary internet in guestrooms. Complimentary Wi-Fi is also available in the lobby and public areas.
- Parking is available on property.
    - Discounted Self-Parking: $30 USD per night
    - Discounted Valet Parking Fee: $35 USD per night

Travel

Air Travel

You are responsible for booking your own air travel.
Airport Option: San Diego International Airport (SAN) is about an 8-minute walk or 5-minute drive from the Sheraton San Diego Hotel & Marina hotel.
Special Airfares: Travel arrangements using the IEEE negotiated air carriers or the carriers of your choice can be made through World Travel, Inc.

- Call in: Between 8:00 AM and 5:30 PM EST, Monday through Friday. Within the US and Canada, call (800) TRY-IEEE, (+1 800 879-4333); and outside of the US and Canada, call +1 717 556-1100.
- Online: Visit their website at http://www.ieee.org/travel.
- Email: Email your request toieee@worldtravelinc.com.

Ground Transportation for Getting Around

Complimentary Airport Shuttle to and from the hotel. The shuttle arrives every 20-25 minutes from 4:45 AM to 1:00 AM, seven days a week. If you are arriving in San Diego, see below for Terminal 1 & 2 shuttle pickup instructions.
Uber/Lyft
Taxi
Discounted Car Rentals: IEEE corporate car rental discounts are available to all attendees. Use discount codes here when calling your preferred car rental company to receive special rates: Avis A606000, Budget X520000, Hertz 61368, and Enterprise NA24IE1.
Airport Shuttle Pickup & Walking Instructions
Driving and Walking Directions from the San Diego International Airport (SAN):

- Shuttle Pickup from Terminal 1
  - After collecting your luggage, follow the "Ground Transportation" signage.
  - Walk across the sky bridge.
  - Take the escalator down to the ground level.
  - Turn right.
  - Cross the taxi/van concrete islands.
  - Walk to 3rd island, marked "Courtesy Vehicles."
  - Wait at any open spot on the curb.

- Shuttle Pickup from Terminal 2
  - After collecting your luggage, walk across the street (toward Taxi/Hotel/Rental Car Shuttles).
  - Walk to the 2nd island (courtesy shuttles/car rental shuttles)
  - Turn left and walk down to area marked 'Courtesy Shuttles'
  - Walking
  - Head southeast on Airport Terminal Road toward Air Lane
  - Turn right onto N Harbor Drive
  - Turn left onto Harbor Island Drive
  - Destination will be on the right. Arrive at Sheraton San Diego Hotel & Marina.

On-site Conference Registration Desk Hours:

Registration will be open in the Main Foyer Bay Tower right outside of the Bell Aire Ballroom - Bay Tower

- Sunday, October 14 7:00 AM - 5:00 PM
- Monday, October 15 7:00 AM - 5:00 PM
- Tuesday, October 16 7:00 AM - 5:00 PM
- Wednesday, October 17 8:00 AM - 5:00 PM

Meeting Locations:

- Sunday: short course will take place in the Bell Aire Ballroom - Bay Tower
- Monday - Primer/tutorials will take place in the Bell Aire Ballroom - Bay Tower (tutorials registrants only)

- Monday - Wednesday - Registration will take place on the 2nd floor in the Foyer outside of the Bel Aire Ballroom
- Monday - Tuesday: Exhibits will take place in Fairbanks Ballroom - Bay Tower

Conference Networking & Social Events:

Several networking events have been arranged to promote informal social interactions among conference participants. Event details are listed below for your reference:

Monday, October 15, 2018: Exhibitor Reception from 5:00 PM to 7:00 PM; Location: Fairbanks Ballroom
Tuesday, October 16, 2018: Exhibitor Luncheon from 11:30 AM to 1:00 PM; Location: Fairbanks Ballroom
Tuesday, October 16, 2018: Conference Banquet from 5:45 PM to 10:00 PM; Location: Tom Han's Lighthouse

Additional Conference Banquet Information:
Tuesday, October 16, 2018:

BCICTS' conference banquet will take place at Tom's Ham's Lighthouse. Tom Ham's Lighthouse is a fully functioning lighthouse and is one of San Diego's best known architectural landmarks. In addition to the lighthouse, Tom Ham's is also famous for its eye-catching views of the San Diego Bay, Coronado Bridge and San Diego skyline. Attendees will also enjoy flavorful menu items in addition to an experience of a lifetime! We will depart the Bay Tower Hotel Lobby at 5:45 pm. The Lighthouse is approximately 8-10 minutes walking distance from the hotel. Please bring a jacket or sweater as the weather may get a little chilly in the evening and also wear comfortable shoes!

Tom Ham's Lighthouse
2150 Harbor Island Drive
San Diego, CA 92101

*Event times are subject to change
6:00 - 6:30 pm: Welcome/Cocktail Hour
6:30 - 8:00 pm: Dinner
8:00 - 9:00 pm: Dessert, Coffee/Tea and Networking!

Meals:
All Meals will be served inside the Fairbanks Ballroom, Bay Tower

Attendee Lounge & Speaker Ready Room:
The Attendee Lounge/Speaker Ready Room will be available inside the Fairbanks Ballroom from 8:00 AM - 5:00 PM daily.

ADDITIONAL INFORMATION

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REGISTRATION Complete registration information is contained in the centerfold of this booklet as well as on the conference's web page (https://bcicts.org) Please use the website to register. The advanced registration deadline is **September 7, 2018**. All conference activities are included in the registration fees (technical sessions, food breaks and the banquet) as well as a USB flash drive with an electronic copy of BCICTS 2018 Proceedings.

OTHER CONFERENCE SOCIAL EVENTS Several events have been arranged to promote informal social interactions among conference participants.

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BCICTS 2018 Short Course and Schedule

Bel Aire Ballroom South

Date: Sunday, October 14, 2018
Time: 7:30 AM - 4:00 PM
Discussion Topic: Phased Arrays and Massive MIMO: Technology and Systems
Speakers:

- Mark Rodwell (UCSB)
- Gabriel Rebeiz (UCSD)
- Amitava Ghoush (Nokia)

7:15 - 7:45 AM Registration and breakfast

7:45 - 8:00 AM Welcome

The' Linh Nguyen and Shahriar Shahramian

Course Overview

Renowned experts from academia and industry will share their views on technology and systems for active antenna systems used in massive MIMO, 5G, and beyond.

8:00 - 10:00 AM

Device, Circuit, and Systems Considerations for Highly Integrated 30-300GHz Wireless Systems

Instructor: Mark Rodwell (UCSB)

Wireless links using mm-wave (30-300GHz) carrier frequencies can support massive spatial multiplexing, hence massive transmission capacities in both endpoint and backhaul links. Imaging systems using higher (100-300GHz) carrier frequencies can provide foul-weather imaging with TV-like resolution, with applications in automobiles and aircraft. These systems will require high-frequency transistors in VLSI, SiGe, and III-V technologies, phased-array transceiver front-ends, and complex silicon RF ICs to form and aim multiple beams and to null or equalize multipath interference. We will review the design and performance of high-frequency transistors, mm-wave ICs, high-frequency packaging, array modules, and mm-wave imaging and spatially multiplexed communications system design.

Mark Rodwell (Ph.D. Stanford University 1988) holds the Doluca Family Endowed Chair in Electrical and Computer Engineering at UCSB. He directs the SRC/DARPA Center for Converged TeraHertz Communications and Sensing. His research group develops nm and THz transistors, and mm-wave and sub-mm-wave integrated circuits and systems. The work of his group and collaborators has been recognized by the 2010 IEEE Sarnoff Award, the 2012 IEEE Marconi Prize Paper Award, the 1997 IEEE Microwave Prize, the 1998 European Microwave Conference Microwave Prize, and the 2009 IEEE IPRM Conference Award.

10:00 - 10:30 AM Break

10:30 - 12:30 PM

Phased-Array Architectures and Demonstrations for 5G: The End of the Marconi Era is Near

Instructor: Gabriel M. Rebeiz (UCSD)

The talk summarizes the different phased-array architectures used and their related packaging for 5G applications: 28 GHz, 39 GHz, 60 GHz and above. Different phased-arrays will be shown together with their performance over frequency, bandwidth, polarization, and scan range. The work will show that it is possible to build state-of-the-art phased-arrays using simple printed-circuit boards and low-cost silicon chips, ushering the era of Gbps Directive Communications and ending the Marconi Era of communication systems based on Mbps broadcast-to-omni-directional antennas.

Gabriel M. Rebeiz is Distinguished Professor, the Wireless Communications Industry Endowed Chair at UCSD, and Member of the National Academy (elected for phased-arrays). He is an IEEE Fellow, and received the IEEE Daniel Nobel Award for his work on RF MEMS, the MTT Microwave Prize (twice for phased-array topics),

the MTT Distinguished Educator Award, IEEE Antennas and Propagation John D. Kraus Award for the mm-wave dielectric lens antenna, and the Harold Wheeler Award for multi-mode phased-array antennas. He also received the Amoco Teaching Award given to the best undergraduate teacher at the University of Michigan, and the Jacobs ECE Teacher of the Year at UCSD. He is considered as one of the fathers of RF MEMS and tunable networks, affordable silicon RFIC phased arrays, and mm-wave and THz antennas. Prof. Rebeiz has graduated nearly 100 PhD students and post-docs, has written 700 IEEE publications, and has been referenced over 35,000 times with an h-index of 82 (one of the highest in the world for RF/microwaves). He was a co-founder of Spectra-Beam (acquired by IDT) and is an advisor to several of the largest commercial and defense companies in the US.

12:30 - 1:30 PM Lunch

1:30 - 3:30 PM
NR Radio Interface for sub 6GHz and mmWave bands

Instructor: Amitava Ghosh (Nokia)

3GPP NR provides a unified, flexible radio interface capable of supporting various 5G verticals such as automotive, healthcare, industry, smart city, etc. In this talk, we will provide an overview of 5G NR radio interface design and will cover advanced technologies for NR such as scalable OFDM numerology, flexible slot structure, beamformed access, advanced channel coding and mmWave technology and how these features enables these 5G verticals. We will also present the system performance of 5G NR both at sub 6GHz and mmWave bands. Finally, the talk will provide an outlook of new features which will be studied in 3GPP Rel-16 and 17.

Amitava Ghosh is a Nokia Fellow and Head, Radio Interface Group at Nokia Bell Labs. He joined Motorola in 1990 after receiving his Ph.D in Electrical Engineering from Southern Methodist University, Dallas. Since joining Motorola, he worked on multiple wireless technologies starting from IS-95, cdma-2000, 1xEV-DV/1XTREME, 1xEV-DO, UMTS, HSPA, 802.16e/WiMAX and 3GPP LTE. He has 60 issued patents, has written multiple book chapters and has authored numerous external and internal technical papers. He is currently working on 3GPP LTE-Advanced and 5G technologies. His research interests are in the area of digital communications, signal processing and wireless communications. He is the recipient of 2016 IEEE Stephen O. Rice and 2017 Neal Shephard prize, member of IEEE Access editorial board and co-author of the book titled “Essentials of LTE and LTE-A”.

3:30 - 4:00 PM Course Evaluation

BCICTS 2018 Primer Course and Schedule

Bel Aire Ballroom South

Date: Monday, October 15, 2018
Time: 7:30 AM - 12:00 PM
Discussion Topic: SiGe Technology and mmW Layout Techniques
Speakers:

- Pascal Chevalier (ST-Microelectronics)
- Shahriar Shahramian (Bell Labs/Nokia)

7:00 - 7:50 AM Registration and breakfast

7:50 - 8:00 AM Welcome

Bruce Green and The' Linh Nguyen

Course Overview

Renowned experts from industry teach present more tutorial and fundamental instruction for those new to the field or wanting a refresher. This will include SiGe technology and mm-wave layout tips and tricks components.

8:00 - 9:40 AM
Fundamentals of High-Speed SiGe BiCMOS Technologies

Instructor: Pascal Chevalier (STMicroelectronics)

Since the qualification in production of the first SiGe BiCMOS technology in a 0.5-µm CMOS node 20 years ago, many high-speed BiCMOS platforms were developed at different locations in various CMOS nodes, to reach today 55nm for the most advanced one. They remain appealing for many applications in spite of the growing attractiveness of CMOS technologies for RF applications during this period. The objective of this primer course is to understand fundamentals of high-speed SiGe BiCMOS technologies. The main focus will be on Si/SiGe Heterojunction Bipolar Transistor (HBT), but topics related to CMOS node and passive devices will be covered as well. The course will start with a review of the figures of merit and related extraction methods involved in SiGe HBT and BiCMOS technology. Advantages and positioning of BiCMOS compared to CMOS will also be shown. The second part will concentrate on high-speed SiGe HBT. Basics on device physics, related trade-offs and transistor architectures will be analyzed. Vertical and lateral scaling of the transistor will be discussed. This part will end with a presentation of SiGe HBT state-of-the-art and a review of different modeling tools used for the development of BiCMOS technologies. The third and last part will begin with a presentation of BiCMOS state-of-the-art. Bipolar / CMOS integration schemes will then be shown and related opportunities and challenges accompanying CMOS scaling will be examined. Fabrication of medium & high-voltage SiGe HBTs and passive devices, with in particular the impact of back-end of line, will also be discussed. The course will be illustrated with examples taken from 0.35-µm to 55-nm SiGe BiCMOS technologies developed by STMicroelectronics.

Pascal Chevalier received the Ph.D. degree in electronics from the University of Lille, France, in 1998 for his work on AlInAs/GaInAs InP-based HEMT. He has worked on BiCMOS technologies for nearly 20 years, starting from 0.35-µm Si BiCMOS at Alcatel Microelectronics, Belgium, to the most recent 55-nm SiGe BiCMOS at STMicroelectronics, France. He led research on advanced RF and millimeter-wave silicon-based devices such as SiGe HBT and Si LDMOS transistors for bulk and partially depleted SOI CMOS derivative technologies. He is currently managing the Mixed Signal (including RF-SOI CMOS) & BiCMOS Technologies R&D team at STMicroelectronics where he is also a Senior Member of the Technical Staff.

9:40 - 10:10 AM Break

10:10 - 11:50 AM
The Art of mm-Wave Layout

Instructor: Shahriar Shahramian (Bell Labs/Nokia)

We live in the golden age of mm-wave ASIC design! With the rise of 5G networks, a massive push for commercialization of mm-wave integrated circuits is underway. This course explores the hidden impairments which are often overlooked or difficult to locate in mm-wave layouts and interconnects. Using real-life fabricated circuit blocks operating in the W-Band and optical circuits operating beyond 100Gb/s, you are invited to search for parasitic capacitive, inductive, resistive and coupled elements which can adversely affect the circuit performance. After the modeling of these elements, simulations demonstrate the impact of the parasitics on bandwidth, center frequency, stability and noise-figure. Using simple and quick modeling techniques, the designers can incorporate various layout effects into their design. Finally, mm-wave techniques at chip level are explored from ground planes to packaging.

Shahriar Shahramian received his Ph.D. degree from University of Toronto in 2010 where he focused on the design of mm-wave data converters and transceivers. Dr. Shahramian has been with the Bell Laboratories division of Alcatel-Lucent (now Nokia), Murray Hill, NJ since 2009 and is currently the Director of the mm-Wave ASIC Research Department. He is also a member of the technical program committee of IEEE Compound Semiconductor Integrated Circuits Symposium (CSICS) and IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS). He is also a guest Editor of the IEEE Journal of Solid-State Circuits (JSSC). His research focus includes the design of mm-wave wireless and wireline integrated circuits. He is the lead designer of several state-of-the-art ASICs for optical coherent and wireless backhaul products at Bell Laboratories. Dr. Shahramian has been the recipient of Ontario Graduate Scholarship, University of Toronto Fellowship and the best paper award at the CSICS Symposium in 2005, 2015 and RFIC Symposium in 2015. He also holds an adjunct associate professor position at Columbia University, has received several teaching awards and is the founder and host of The Signal Path educational video series.

11:50 - 12:00 PM Course Evaluation

INTRODUCTORY REMARKS AND PLENARY

WELCOME AND ANNOUNCEMENTS
1:10 - 1:40 PM - **Bell Aire Ballroom**

PLENARY

Monday 1:40 PM - Bell Aire Ballroom
Session Chair: Pete Zampardi, *Qorvo*
Co-chair: Sorin Voinigescu, *University of Toronto*

1:40 PM - 2:10 PM - Current Status of Terahertz Integrated Circuits - from Components to Systems
Ullrich R. Pfeiffer, Ritesh Jain, Janusz Grzyb, Stefan Malz, Phillip Hillger, and Pedro Rodríguez-Vázquez
Institute for High-Frequency and Communication Technology,
University of Wuppertal, Wuppertal, Germany

2:10 PM - 2:40 PM - Indium Phosphide Photonic Integrated Circuits: Technology and Applications
Jonathan Klamkin, Hongwei Zhao, Bowen Song, Yuan Liu, Brandon Isaac, and Larry Coldren
University of California Santa Barbara Santa Barbara, CA, USA

2:40 PM - 3:10 PM - The RF Sampler: Chip-scale Frequency Conversion and Filtering Enabling Affordable Element-level Digital Beamforming
Matthew Morton[1], Yan Chen[1], Alyosha Molnar[2], Edward Szoka[2], and Robin Ying[2]
[1]Raytheon Company, 50 Apple Hill Drive, Tewksbury, MA, USA
[2]Cornell University, Phillips Hall, Ithaca, NY, USA

3:10 PM - 3:40 PM - Technology Positioning for mmWave Applications: 130/90nm SiGe BiCMOS vs. 28nm RFCMOS
Alvin Joseph, Vibhor Jain, Shih Ni Ong[1], Randy Wolf, Suh Fei Lim[1], and Jagar Singh[2]
GLOBALFOUNDRIES, Essex Junction, VT, USA
[1]GLOBALFOUNDRIES, Singapore
[2]GLOBALFOUNDRIES, Malta, NY USA

CONFERENCE PROGRAM

1. Optical Communications

Monday 4:00 PM - ***Bell Aire Ballroom North***
Session Chair: Kumar Lakshmikumar, *Cisco Systems*
Co-Chair: Patrice Gamand, *XLIM, University Limoges*

1.1 (Invited)
4:00-4:30 PM - Analog Optical RF-Links for Large Radio Telescopes
Jonas Weiss
IBM Research - Zurich, Switzerland

1.2
4:30-4:50 PM - A 256-Gbps PAM-4 Signal Generator IC in 0.25-μm InP DHBT Technology

Munehiko Nagatani[1], Hitoshi Wakita[1], Teruo Jyo[1], Miwa Mutoh[1], Minoru Ida[1], Sorin P. Voinigescu[1*,2], and Hideyuki Nosaka[1]
[1]NTT Device Technology Laboratories, NTT Corporation, 3-1 Morinosato-Wakamiya, Atsugi, Kanagawa, 243-0198, Japan
[2]ECE Department, University of Toronto, Toronto, ON, M5S 3G4, Canada

1.3
4:50 -5:10 PM - A 3D-Integrated 56 Gb/s NRZ/PAM4 Reconfigurable Segmented Mach-Zehnder Modulator-Based Si-Photonics Transmitter
Cheng Li[1], Kunzhi Yu[1,2], Jinsoo Rhim[1], Kehan Zhu[1], Nan Qi[1], Marco Fiorentino[1], Thierry Pinguet[3], Mark Peterson[3], Vishal Saxena[4], and Samuel Palermo[3]
[1]Hewlett Packard Labs, Palo Alto, CA, USA
[2]Texas A&M University, College Station, TX, USA,
[3]Luxtera, Inc., Carlsbad, CA, USA,
[4]University of Idaho, Moscow, ID, USA

2. Applications of GaN HEMT Modeling

Monday 4:00 PM - ***Bell Aire Ballroom South***
Session Chair: Masaya Iwamoto, *Keysight Technologies*
Co-Chair: Mikael Garcia, *Analog Devices*

2.1 (Invited)
4:00-4:30 PM - Nonlinear Embedding of FET Devices for High Efficiency Power Amplifier Design
Haedong Jang, Zulhazmi Mokhti, Björn Herrmann, and Richard Wilson
Wolfspeed CREE Inc., Morgan Hill, CA, USA

2.2
4:30-4:50 PM - Analysis of Gate-Voltage Clipping Behavior on Class-F and Inverse Class-F Amplifiers
Hiroshi Yamamoto[1], Ken Kikuchi[1], Norihiko Ui[1], Kazutaka Inoue[1], Valeria Vadalà[2], Gianni Bosi[2], Antonio Raffo[2], and Giorgio Vannini[2]
[1]*Transmission Devices Laboratory, Sumitomo Electric Industries, Ltd. 1 Taya-cho, Sakae-ku, Yokohama, Kanagawa 244-8588, Japan*
[2]*Department of Engineering*
University of Ferrara, via Saragat 1, Ferrara, 44122, Italy

2.3
4:50 -5:10 PM - Ka-band GaN Large-Signal Model Considering Trap Effect on Non-linear Capacitance by Using Transient S-parameters Measurement
Yutaro Yamaguchi[1], Tomohiro Otsuka[1], Masatake Hangai[1], Shintaro Shinjo[1], and Toshiyuki Oishi[2]
[1]Information Technology R&D Center, Mitsubishi Electric Corporation, 5-1-1 Ofuna, Kamakura, Kanagawa, 247-8501, Japan
[2]Saga University, 1 Honjo-machi, Saga, Saga, 840-8502, Japan

3. Data Converter Circuits

Tuesday 8:00 AM - ***Bell Aire Ballroom North***
Session Chair: Yuriy Greshishchev, *Ciena*
Co-Chair: Craig Steinbeiser, *Qorvo*

3.1 (Student)

8:00-8:30 AM - A 2x-Oversampling, 128-GS/s 5-bit Flash ADC for 64-GBaud Applications
Alireza Zandieh*, Peter Schvan†, and Sorin P. Voinigescu*
**ECE Department, University of Toronto, Toronto, ON, Canada*
†Ciena Corporation, Ottawa, ON, Canada

3.2 (Student)
8:30-8:50 AM - A 25.6-GS/s 40-GHz 1-dB BW Current-Mode Track-and-Hold Circuit with more than 5-ENOB
Xuan-Quang Du, Markus Grözing and Manfred Berroth
Institute of Electrical and Optical Communications Enginering University of Stuttgart, Stuttgart, Germany

3.3 (Student)
8:50 -9:10 AM - A 12 GS/s Track-and-Hold Amplifier with Track Mode Masking Achieving 12 dBm P1dB and 24 dBm IIP3 in 55 nm SiGe-BiCMOS
P. Thomas*, M. Buck*, M. Grözing*, M. Berroth*,J. Rauscher†, M. Epp† and M. Schlumpp†
**Inst. of Electrical and Optical Communications Engineering University of Stuttgart,Stuttgart, Germany*
†HENSOLDT Sensors GmbH,Ulm, Germany

4. State-of-the-Art SiGe BiCMOS

Tuesday 8:00 AM - ***Bell Aire Ballroom South***
Session Chair: Jay John, *NXP Semiconductors*
Co-Chair: Mattias Dahlstrom, *Texas Instruments*

4.1 (Invited)
8:00-8:30 AM - SiGe BiCMOS Current Status and Future Trends in Europe
Pascal CHEVALIER[1], Wolfgang LIEBL[2], Holger RÜCKER[3], Alexis GAUTHIER[1], Dirk MANGER[4], Bernd HEINEMANN[3], Grégory AVENIER[1], Josef BÖCK[5]
1) STMicroelectronics Crolles, France
2) Infineon Technologies Regensburg, Germany
3) IHP Frankfurt (Oder), Germany
4) Infineon Technologies Dresden, Germany
5) Infineon Technologies Neubiberg, Germany

4.2 (Student)
8:30-8:50 AM - 450 GHz f_T SiGe:C HBT featuring an implanted collector in a 55-nm CMOS node
A. Gauthier[1,2], J. Borrel[1], P. Chevalier[1], G. Avenier[1], A. Montagné[1], M. Juhel[1], R. Duru[1], L.-R. Clément[1], C. Borowiak[1], M. Buczko[1] and C. Gaquière[2]
1) STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France
2) IEMN, UMR 8520, USTL, Avenue Poincaré - BP69, 59652 Villeneuve d'Ascq, France

4.3
8:50 -9:10 AM - Integration of SiGe HBT with f_T = 305GHz, f_{max} = 537GHz in 130nm and 90nm CMOS
4. Manger[1], W. Liebl[2], S. Boguth[2], B. Binder[1], K. Aufinger[2], C. Dahl[1], C. Hengst[1], S. Majied[2], A. Pribil[1], J. Oestreich[1], S. Rohmfeld[1], S. Rothenhaeusser[1], 4. Tschumakow[1], J. Boeck[2]
1) Infineon Technologies Dresden GmbH, 01099 Dresden, Germany
2) Infineon Technologies AG, 81726 Munich, Germany

5. 5G Components and Systems

Tuesday 9:30 AM - ***Bell Aire Ballroom North***
Session Chair: Mike Roberg, *Qorvo*
Co-Chair: Tomoya Kaneko, *NEC Corporation*

5.1 (Invited)
9:30-10:00 AM - Scaling Millimeter-wave Phased Arrays: Challenges and Solutions
Alberto Valdes-Garcia, Bodhisatwa Sadhu, Xiaoxiong Gu, and Jean-Olivier Plouchart
IBM T. J. Watson Research Center, Yorktown Heights, NY, USA

5.2 (Student)
10:00-10:20 AM - A 28-GHz, 18-dBm, 48% PAE Stacked-FET Power Amplifier with Coupled-Inductor Neutralization in 45-nm SOI CMOS
Kang Ning, James F. Buckwalter
University of California Santa Barbara, Santa Barbara, CA, USA

5.3
10:20 -10:40 AM - A 2-6 GHz, 45 dBm peak power T/R SPDT switch for 5G mMIMO Applications
Venkata Malladi, Mike Fraser, Joseph Staudinger, Mario Bokatius, Monte Miller
NXP Semiconductors, Chandler, AZ, USA

6. Advances in GaN Modeling

Tuesday 9:30 AM - ***Bell Aire Ballroom South***
Session Chair: Yueying Liu, *Wolfspeed*
Co-Chair: Subrata Halder, *Qorvo*

6.1 (Invited)
9:30-10:00 AM - Non-linear RF Modeling of GaN HEMTs with Industry Standard ASM GaN
Sourabh Khandelwal, Yogesh S. Chauhan*, Jason Hodges, and Sayed Ali Albahrani
School of Engineering, Macquarie University, Sydney, Australia
**Indian Institute of Technology, Kanpur, India*

6.2
10:00-10:20 AM - Improved Charge Modeling of Field-plate Enhanced AlGaN/GaN HEMT Devices Using a Physics Based Compact Model
Improved Charge Modeling of Field-plate Enhanced AlGaN/GaN HEMT Devices Using a Physics Based Compact Model
Kevin Kellogg, Sourabh Khandelwal*, Neil Craig**, and Larry Dunleavy
Modelithics, Tampa, FL, USA
**Macquarie University, Sydney, Australia*
***Qorvo USA*

6.3 (Student)
10:20 -10:40 AM - Incorporation of the Virtual Gate Effect and Consequences of its Neglect in the Simulation of ON-state ID-VDS Curves of AlGaN/GaN HEMTs
Pradeep Dasari, Chandan Sharma*, and Shreepad Karmalkar

Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai, India, 600036
**Solid State Physics Laboratory, DRDO lab, New Delhi, India, 110054*

7. High Frequency Characterization

Tuesday 11:00 AM - ***Bell Aire Ballroom North***
Session Chair: Andrej Rumiantsev, *MPI Corporation*
Co-Chair: Michael Schroter, *TU Dresden and UCSD*

7.1 (Invited)
11:00-11:30 AM - On-Wafer Transistor Characterization to 750 GHz -the approach, results, and pitfalls
Dylan F. Williams, Jerome Cheron, Benjamin Jamroz, Richard Chamberlin
National Institute of Standards and Technology, Boulder, CO, USA

7.2 (Student)
11:30 -11:50 AM - Iterative De-embedding and Extracted Maximum Oscillation Frequency fMAX in mm-Wave InP DHBTs: The Impact of Device Dimensions on Extraction Errors
W. Quan, A. M. Arabhavi, R. Flueckiger, O. Ostinelli, and C.R. Bolognesi*
Millimeter-Wave Electronics Group
ETH-Zürich
Gloriastrasse 35, 8092 Zurich, Switzerland

8. Extreme Bandwidth mmW Circuits

Tuesday 11:00 AM - ***Bell Aire Ballroom South***
Session Chair: Nils Pohl, *Ruhr-University Bochum*
Co-Chair: Vadim Issakov, *Infineon*

8.1
11:00-11:20 AM - A Low-Power Triple-Loop Feedback Broadband LNA in a 130 nm SiGe BiCMOS Technology
Badou Sene [1;2], Vadim Issakov[1]
[1]Infineon Technologies AG, Am Campeon 1-12, D-85579 Neubiberg, Germany
[2]Ruhr-University Bochum, Universit¨atsstr. 150, D-44780 Bochum

8.2 (Student)
11:20 -11:40 AM - 1.5-54 GHz High Dynamic Range LNA and Mixer Combination for a MIMO Radar Application
Mantas Sakalas, Niko Joram, Frank Ellinger
Chair for Circuit Design and Network Theory, Technische Universität Dresden, Germany

8.3 (Student)
11:40 AM-12:00 PM - A Low Insertion-Loss 10-110 GHz Digitally Tunable SPST Switch in 22 nm FD-SOI CMOS
Radu Ciocoveanu[1,2], Robert Weigel[2], Amelie Hagelauer[2] and Vadim Issakov[1]
[1]Infineon Technologies AG, Neubiberg, Germany
[2]Friedrich-Alexander University Erlangen-Nuremberg (FAU), Erlangen, Germany

9. Emerging Compound Semiconductor Device Technology

Tuesday 1:10 PM - ***Bell Aire Ballroom North***
Session Chair: Carl Dohrman, *Northrup Grumman Innovation Systems*
Co-Chair: Kazutaka Inoue, *Sumitomo Electric Industries, Ltd.*

9.1 (Invited)
1:10-1:40 PM - Materials, Processes, and Markets for Monolithic III-V Devices in Silicon Integrated Circuits
E.A. Fitzgerald
Dept of Materials Science and Engineering, MIT
Low Energy Electronic Systems, Singapore MIT Alliance for Research and Technology
Cambridge, MA and Singapore, Singapore

9.2 (Student)
1:40-2:00 PM - Scaling of InP/GaAsSb DHBTs: A Simultaneous fT/fMAX = 463/829 GHz in a 10 μm Long Emitter
A. M. ARABHAVI, W. QUAN, O. OSTILELLI, AND C.R. BOLOGNESI*
Millimeter-Wave Electronics Group,
ETH-Zurich,
Gloriastrasse 35, 8092 Zurich, Switzerland

9.3 (Invited)
2:00-2:30 PM - GaN HEMT for Space Applications
Tomio SATOH, Ken OSAWA and Atsushi NITTA
SUMITOMO ELECTRIC DEVICE INNOVATIONS, INC.
1000 Kamisukiawara, Showa, Nakakoma, Yamanashi, 409-3883 JAPAN

10. Power Amplifiers and Supporting Circuits

Tuesday 1:10 PM - ***Bell Aire Ballroom South***
Session Chair: Taylor Barton, *University of Colorado Boulder*
Co-Chair: Jon Mooney, *Raytheon (Dallas, TX)*

10.1
1:10-1:30 PM - 40W Ka-Band Single and Dual Output GaN MMIC Power Amplifiers on SiC
Michael Roberg, Thi Ri Mya Kywe, Matthew Irvine, Orlando Marrufo and Sabyasachi Nayak
Qorvo, Inc. - Infrastructure and Defense Products
Richardson, TX, USA

10.2 (Student)
1:30-1:50 PM - A 4-W K-Band 40% PAE Three-Stage MMIC Power Amplifier
Maxwell R. Duffy[*], Gregor Lasser[*], Michael Roberg[†], and Zoya Popović[*]
[*]*Department of Electrical, Computer, and Energy Engineering, University of Colorado, Boulder, CO, USA*
†Infrastructure and Defense Products, Qorvo, Richardson, TX, USA

10.3
1:50-2:10 PM - A 200 MHz Bandwidth GaAs Switch-mode Supply Modulator
Tatsuya Soma, Shinichi Hori, Kazuaki Kunihiro

System Platform Research Laboratories
NEC Corporation
Kawasaki, Kanagawa, 211-8666, Japan

10.4
2:10-2:30 PM - Monolithic Attenuator/Limiter using Nonlinear Resistors
Scott Schafer, Michael Roberg
Qorvo, Inc. - Infrastructure and Defense Products
Richardson, TX, USA

11. Sub-Terahertz Amplifiers and Technology

Tuesday 2:50 PM - ***Bell Aire Ballroom North***
Session Chair: Marc Rocchi, *OMMIC*
Co-Chair: Miro Micovic, *HRL Laboratories*

11.1
2:50-3:10 PM - High Gain 220 - 275 GHz Amplifier MMICs based on metamorphic 20 nm InGaAs MOSFET Technology
Axel.Tessmann, A. Leuther, F. Heinz, F. Bernhardt, H. Massler
Fraunhofer Institute for Applied Solid State Physics (IAF), Tullastr. 72, 79108 Freiburg, Germany

11.2
3:10-3:30 PM - Wideband Amplifier with Integrated Power Detector for 100 GHz to 200 GHz mm-Wave Applications
Paul Stärke, Vincent Rieß, Corrado Carta and Frank Ellinger
Chair for Circuit Design and Network Theory
Technische Universität Dresden
01069 Dresden, Germany

11.3 (Student)
3:30-3:50 PM - 10.9-16.2 mW Series-Connected Power Amplifiers Designed at 326 GHz using 130 nm InP HBT Technology
Ahmed S. H. Ahmed1, Arda Simsek1, Miguel Urteaga2, Mark J. W. Rodwell1
1ECE Department, University of California, Santa Barbara, Santa Barbara, CA, USA
2Teledyne Scientific and Imaging, 1049 Camino Dos Rios, Thousand Oaks, CA, USA

11.4 (Invited)
3:50-4:20 PM - FinFET for mmWave - Technology and Circuit Design Challenges
Steven Callender, Woorim Shin, Hyung-jin Lee, Stefano Pellerano, Christopher D. Hull
Intel Corporation, Hillsboro, OR, USA

12. Silicon Based Device Physics and Reliability

Tuesday 2:50 PM - ***Bell Aire Ballroom South***
Session Chair: Guanghai Ding, *Analog Devices*
Co-Chair: Jonggook Kim, *Texas Instruments*

12.1 (Invited)
2:50-3:20 PM - Carrier Transport in BJTs: From ballistic to diffusive and off-equilibrium
Mark Lundstrom

School of Electrical and Computer Engineering
Purdue University
West Lafayette, IN, USA

12.2
3:20 -3:40 PM - Impact of Emitter Width Scaling on Performance and Ruggedness of SiGe HBTs for PA Applications
Saurabh Sirohi, Vibhor Jain, Ajay Raman, Bhargava Nukala, Elan Veeramani, James W. Adkisson, and Alvin Joseph
GLOBALFOUNDRIES, 1000 River Street, Essex Junction, VT, USA

12.3
3:40 -4:00 PM - Noise Figure Characterization of Horizontal Current Bipolar Transistor (HCBT)
Josip Žilak, Marko Koričić, Željko Osrečki, Marko Šimić and Tomislav Suligoj
Micro and Nano Electronics Laboratory, Department of Electronics
Faculty of Electrical Engineering and Computing, University of Zagreb
HR-10000, Zagreb, Croatia

12.4 (Student)
4:00-4:20 PM - Emitter-Base Profile Optimization of SiGe HBTs for Improved Thermal Stability and Frequency Response at Low-Bias Currents
Uppili S. Raghunathan, Brian R. Wier, Zachary E. Fleetwood, Michael A. Oakley, Vibhor Jain*, and John D. Cressler
School of ECE, 777 Atlantic Drive, N.W., Georgia Tech, Atlanta, GA, USA
**GLOBALFOUNDRIES, Essex Junction, VT, USA*

13. Advanced Circuits in SiGe Technology

Wednesday 9:00 AM - ***Bell Aire Ballroom North***
Session Chair: Tony Quach, *Air Force Research Laboratory*
Co-Chair: Nabil El-Hinnawy, *TowerJazz*

13.1
9:00-9:20 AM - A 6 kV ESD-protected Low-Power 24GHz LNA for Radar Applications in SiGe BiCMOS
Vadim Issakov[1], Sebastian Kehl-Waas[1], Radu Ciocoveanu[1;2], Werner Simburger[1], Angelika Geiselbrechtinger[1]
1 Infineon Technologies AG, Am Campeon 1-15, D-85579 Neubiberg, Germany
2 University Erlangen-Nuremberg, Cauerstr 9, D-91058 Erlangen, Germany

13.2 (Student)
9:20 -9:40 AM -A Packaged Single-Ended K-Band SiGe LNA with 2.14 dB Mean Noise Figure
Abdurrahman H. Aljuhani[1,3], Tumay Kanar[2], and Gabriel 13. Rebeiz[1]
1 UC San Diego, La Jolla, CA, USA
2 Integrated Device Technology, San Diego, CA, USA
3 King Abdulaziz City for Science and Technology, Riyadh, Saudi Arabia

13.3 (Student)
9:40 -10:00 AM - A 1-20 GHz, High-Efficiency Distributed Stacked SiGe Power Amplifier

Sunil Rao, Tianyu Chang, Ickhyun Song, Moon-Kyu Cho, and John D. Cressler
School of Electrical and Computer Engineering, Georgia Tech
777 Atlantic Drive N.W. Atlanta, GA USA

13.4 (Student)
10:00 -10:20 AM - Using SiGe-on-SOI HBTs to Build 300°C Capable Analog Circuits
Anup P. Omprakash[1], Adrian Ildefonso[1], George Tzintzarov[1], Jeffrey Babcock[2], Rajarshi Mukhopadhyay[2], and John D. Cressler[1]
1 School of Electrical and Computer Engineering, 777 Atlantic Drive, NW, Georgia Tech, Atlanta, GA, USA
2 Texas Instruments, Dallas, TX, USA

14. Silicon Modeling

Wednesday 9:00 AM - ***Bell Aire Ballroom South***
Session Chair: Breandán Ó hAnnaidh, *ADI*
Co-Chair: Kai Kwok, *Skyworks*

14.1 (Invited)
9:00-9:30 AM - SiGe HBT PA design for 5G (28 GHz and beyond) - Modeling and Design Challenges
Mark P. van der Heijden and Andries J. Scholten
BL Smart Antenna Solutions NXP Semiconductors Eindhoven, The Netherlands
Technology & Operations NXP Semiconductors Eindhoven, The Netherlands

14.2 (Student)
9:30 -9:50 AM - Revisiting Safe Operating Area: SiGe HBT Aging Models for Reliability-Aware Circuit Design
Brian R. Wier, Rafael Perez Martinez, Uppili S. Raghunathan, Hanbin Ying,
Saeed Zeinolabedinzadeh, and John D. Cressler
School of Electrical and Computer Engineering
777 Atlantic Drive, NW, Georgia Tech, Atlanta, GA, USA

14.3
9:50 -10:10 AM - Modeling high-current effects in bipolar transistors: A theory review
M. Schroter1,2, S. Falk1
1Chair for Electron Devices and Integrated Circuits, TU Dresden, Germany;
2ECE Dept., UC San Diego, La Jolla, CA, USA

15. mm-Wave Transceivers

Wednesday 10:40 AM - ***Bell Aire Ballroom North***
Session Chair: Shahriar Shahramian, *Nokia - Bell Labs*
Co-Chair: Kazuya Yamamoto, *Mitsubishi Electric Corporation*

15.1 (Student)
10:40-11:00 AM - A V-Band SiGe Image-Reject Receiver Front-End for Atmospheric Remote Sensing
Milad Frounchi[1], Chris Coen[2], Clifford DY Cheon[1], Nelson Lourenco[2], Wyman Williams[2], and John D. Cressler[1]
1 School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA
2 Advanced Concepts Laboratory, Georgia Tech Research Institute, Atlanta, GA, USA

15.2 (Student)
11:00-11:20 AM - A 220 GHz OOK Outphasing Transmitter in 130-nm BiCMOS Technology
Kefei Wu[1,2], Mona Hella[1]
1 Rensselaer Polytechnic Institute, Troy, New York, USA
2 Analog Devices Inc., Beaverton, OR, USA

15.3 (Student)
11:20-11:40 AM - A 140 GHz MIMO Transceiver in 45 nm SOI CMOS
Arda Simsek[1], Seong-Kyun Kim[2], and Mark J. W. Rodwell[1]
1 ECE Department, University of California, Santa Barbara, CA, USA
2 Teledyne Scientific and Imaging, Thousand Oaks, CA, USA

15.4
11:40 AM-12:00 PM - Integrated 220-260 GHz Radar Frontend
Thomas Merkle, Sandrine Wagner, Axel Tessmann, Michael Kuri, Hermann Massler, Arnulf Leuther
Fraunhofer Institute for Applied Solid State Physics (IAF) Freiburg, 79108, Germany

16. GaN Devices and Packaging

Wednesday 10:40 AM - ***Bell Aire Ballroom South***
Session Chair: Sansaptak Dasgupta, *Intel*
Co-Chair: Parrish Ralston, *Northrup Grumman Electronic Systems*

16.1 (Invited)
10:40-11:10 AM - 650 Volt GaN: Highest Quality-Highest Performance Drives Market RampSensing
Parikha, Y-F. Wua, L. Shena, J. Grittersa, T. Hosodab, R. Barra,K. Smitha, K. Shonob, J. McKaya, H. Clementa, S. Chowdhurya, S. Yea a, 16. Smitha, L. McCarthya, R. Birkhahna, 16. Zuka, Y. Asaib.
a Transphorm Inc., 75 Castilian Drive, Goleta, CA, USA,
b Transphorm Japan, 2-5-15 Shin-Yokohama, Kohoku-ku, Yokohama, Japan.

16.2
11:10-11:30 AM - Leak-Proof Packaging for GaN Chip with Controlled Thermal Spreading and Transients
Yasuo Saito1, Tatsuhiko Aizawa2, Kenji Wasa1, Yoshiro Nogami3
1 Matsugase 3400, Chuo Denshi Kougyo, Co. Ltd., CDK; Kumamoto, Japan
2 Shibaura 3-9-14; Shibaura Institute of Technology, SIT; Tokyo 108-8548, Japan
3 Izumio 6-2-19, Thermo-Graphitics, Co. Ltd., TGC; Osaka 551-0031, Japan

16.3
11:30-11:50 AM - Analysis of Breakdown Characteristics of AlGaN/GaN HEMTs with Low-k/High-k Double Passivation Layers
Kai Nakamura, Hideyuki Hanawa, and Kazushige Horio*
Faculty of systems Engineering, Shibaura Institute of Technology, Japan

17. Late News 1

Wednesday 1:10 PM - ***Bell Aire Ballroom North***

Session Chair: Peter Zampardi, *Qorvo*
Co-Chair: Doug Weiser, *Texas Instruments*

17.1
1:10-1:30 PM - On the use of drift-diffusion and hydrodynamic transport models for simulating the negative differential mobility effect
G. Wedel, T. Nardmann, M. Schröter
Chair for Electron Devices and Integrated Circuits, TU Dresden, Germany

17.2
1:30-1:50 PM - Quantification of Dopant Profiles in SiGe HBT Devices
Eric J. Jones[1], Jonathan Poplawsky[2], Donavan Leonard[2], Keith Chung[1], Kevin Mercurio[1], Paul Brabant[1], Thomas Adam[1], Patrick B. Shea[1], Thomas Knight[1]
1) Northrop Grumman Corporation, Linthicum, MD, USA
2) Center for Nanophase Materials Science, Oakridge National Laboratories, Oakridge, TN, USA

17.3
1:50-2:10 PM - Equivalent Circuit Modelling and Parameter Extraction of GaN HEMT Gate Lag Inducing ACLR Degradation of TDD-LTE BTS PA
Toshihiro Shimoda, Yoji Murao, Tomoya Kaneko
NEC Corporation, Japan

18. Late News 2

Wednesday 1:10 PM - ***Bell Aire Ballroom South***
Session Chair: Sorin Voinigescu, *University of Toronto*
Co-Chair: TBD

18.1 (Student)
1:10-1:30 PM - A Crystal-Less Programmable Clock Generator With RC-LC Hybrid Oscillator for GHz Applications in 14 nm FinFET CMOS
Jeongho Hwang1, Gyu-Seob Jeong1, Sang-Hyeok Chu2, Wooseok Kim2, Taeik Kim2, and Deog-Kyoon Jeong1,
1 Seoul National University
2 Samsung Electronics

18.2 (Student)
1:30-1:50 PM - Large-Swing 22nm Si/SiGe FDSOI Stacked Cascodes for 56GBaud Drivers and 5G PAs
M. Sadegh Dadash[1], David Harame[2], and Sorin P. Voinigescu[1]
1 ECE, University of Toronto, Toronto, ON, M5S 3G4, Canada
2 GlobalFoundries, Dresden, Germany

18.3 (Student)
1:50-2:10 PM - 128-GS/s ADC Front-End with over 60-GHz Input Bandwidth in 22-nm Si/SiGe FDSOI CMOS
Alireza Zandieh[1], Naftali Weiss[1], The'Linh Nguyen[2], David Harame[3], and Sorin P. Voinigescu[1]
1 ECE, University of Toronto, Toronto, ON, M5S 3G4, Canada
2 Finisar Corporation, Sunnyvale, CA, USA
3 GlobalFoundries, Dresden, Germany

18.4 (Student)
2:10-2:30 PM - A DC-60 GHz I/Q Modulator in 45 nm SOI CMOS for Ultra-Wideband 5G Radios
Hasan Al-Rubaye and Gabriel M. Rebeiz
Department of Electrical and Computer Engineering
University of California at San Diego
La Jolla, CA, USA

19. Late News 3

Wednesday 2:50 PM - ***Bell Aire Ballroom***
Session Chair: Brian Moser, *Qorvo*
Co-Chair: Bruce Green, *NXP*

19.1
2:50-3:10 PM - 40V High Side PSI5 Transceiver with 65dBµV Conducted Emission Level in a BiCMOS Process
S.N. Easwaran, A. Chen, T. Duryea, D. Rollman
Texas Instruments Inc, 12500, TI BLVD, Dallas, Texas, USA.

19.2
3:10-3:30 PM - AC-Stacked Power Amplifier for APT/ET LTE HPUE Applications
Kazuo Watanabe, Satoshi Tanaka, Masatoshi Hase, Yuuri Honda, Yusuke Tanaka, and Satoshi Arayashiki
Murata Manufacturing Co., Ltd. Kyoto, Japan

EXECUTIVE COMMITTEE

Brian Moser	Qorvo, Symposium Co-Chair
Peter Magnee	NXP Semiconductors, Symposium Co-Chair
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Frank van Vliet	TNO
John Wood	Obsidian Microwave
Simon Wood	WolfSpeed
Chenggang (CG) Xie	Rockwell Collins, INC Adv Technology Center
Jane Xu	Skyworks
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mm-Wave and THz ICs

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High Speed Digital, Mixed-Signal, and Optoelectronic ICs

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Candi Wooldridge	MP Associates, Inc.
Jessica Lotito	IEEE Electron Devices Society
Jim Skowrenski	IEEE Electron Devices Society
Sherry Russ Sills	IEEE Meetings, Conferences and Events

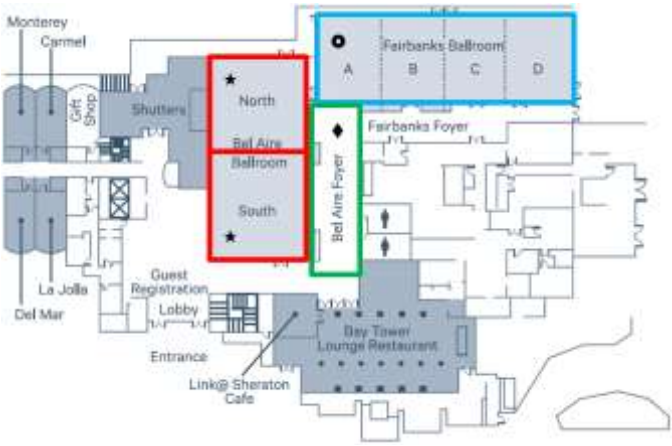
MEETING DIAGRAM & LOCAL INFORMATION

Sheraton San Diego Hotel and Marina

All conference meeting sessions will be held on the Bay Tower Level Lobby Level.

★Short Course, Primer, Technical Sessions

♦Registration Desk **⭘Exhibitor Space**



Local Directory:

7 Dining Options inside the Hotel:

- Bay Tower Lounge
- Harbor's Edge
- Harbor and Vine
- Link@Sheraton Café
- *Quinn's Ale House - TOP Pick
- Marina Market and Café
- Shoreline Restaurant

Dining

Below are recommended restaurant nearby to the hotel:

- Island Prime Restaurant
- Barbusa
- Coasterra
- CUCINA Urbana
- Craft & Commerce
- Volcano Rabbit
- Leroy's Kitchen + Lounge
- Kettner Exchange
- Papanani's Deli & Sundries
- Tom Ham's Lighthouse
- Blue Water Seafood Market & Grill

Here are some of the fun things to do during your stay in San Diego.

- Balboa Park
- Gaslamp Quarter

- Petco Park
- San Diego Zoo & Safari Park
- SeaWorld San Diego
- USS Midway Museum
- Coronado Beach
- Torrey Pines State Reserve
- Cabrillo National Monument
- Maritime Museum of San Diego
- Mission Beach and Pacific Beach
- Sunset Cliffs
- La Jolla
- Little Italy
- Hollywood Casino
- Sycuan Casino
- Shopping: Seaport Village, Horton Plaza, Fashion Valley Mall, Mission Valley Mall

Nearby Destinations:

- Marina Area 0.0 km/0.0 miles
- Little Italy 3.4 km/2.1 miles
- Liberty Station 5.5 km/3.4 miles
- Tijuana, Mexico 29.0 km/18.0 mile

Recreation:

- Note: Bike rentals and tours can also be reserved onsite at the Sheraton on the dock in back of the Marina Tower.
- Sports Arena 7.4 km/4.6 miles
- Petco Park 7.7 km/4.8 miles
- San Diego Zoo 9.0 km/5.6 miles
- Sea World Park 11.4 km/7.1 miles
- Mission Beach 12.2 km/7.6 miles
- Qualcomm Stadium 15.9 km/9.9 miles
- LEGOLAND® California Resort 54.7 km/34.0 miles
- San Diego Wild Animal Park 59.5 km/37.0 miles

CALL FOR PAPERS

2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)

November 3-6, 2019
Loew's Vanderbilt Hotel, Nashville, TN, USA

INTEGRATED CIRCUITS and DEVICES in
GaAs, InP, GaN, SiGe, and other compound semiconductor and CMOS technologies

Sponsored by the IEEE Electron Devices Society, Technically co-sponsored by the Solid State Circuits Society and the Microwave Theory & Techniques Society

2019 BCICTS Symposium

The 2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) is the IEEE-approved merger of the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) and the Compound Semiconductor IC Symposium (CSICS). BCICTS is the forum for developments in bipolar, BiCMOS, and com-pound semiconductor circuits, devices, and technology. Coverage includes all aspects of the technology, from materials, device fabrication, device phenomena, TCAD modeling, compact modeling, integrated circuit design, testing, and system applications. A wide range of integrated circuit technologies are covered including CMOS, bipolar and field-effect transistors realized in materials such as SiGe, GaAs, GaN, InP, SiC. The latest results in wireless, analog, RF, microwave, high-speed digital, mixed signal, optoelectronic, millimeter wave, and THz integrated circuits are embraced. Subject area groupings are:

HIGH-SPEED DIGITAL, MIXED-SIGNAL, AND OPTOELECTRONIC ICs Mixed analog/digital ICs - Digital ICs - (high-speed) DACs and ADCs - Networking ICs, MUX/DEMUX, Clock and data recovery, Decision circuits, Equalizers - Optical data links, Laser and modulator drivers, optoelectronics and photonics ICs

ANALOG, RF, AND MICROWAVE ICs
Op amps - Voltage references and regulators - Integrated filters - Sensors and actuators - RF circuits and systems - Radio and transceiver subsystems - LNAs - AGCs - Mixers - Voltage controlled oscillators - Frequency synthesizers - Power amplifiers - RF switches - Noise and distortion suppression - RF Packaging - Integrated RF passives. Analog, RF, power conversion, High-voltage ICs - Biomedical electronics - Power Management ICs - Energy harvesting ICs - Motor controls - Analog subsystems within a VLSI chip - Packaging of high-performance ICs.

mm-WAVE AND THZ ICs
Millimeter - wave circuits and systems - THz circuits and systems. MM-Wave switches and amplifiers. Phased-array antenna circuits

DEVICE PHYSICS:
New device physics phenomena in Si, SiGe, SiC, GaN, MOS, and III-V HBTs and FETs - Device design issues and scaling limits - Hot electron effects and reliability physics - Transport and high field phenomena - Noise - Linearity/Distortion - Novel measurement techniques - Operation in extreme environments (low/high temperatures, radiation effects), and ESD phenomena.

MODELING AND SIMULATION

Improved silicon-based BJT and HBT models and physics-based modelling techniques - Improved III-V HBT and FET models and physics-based modelling techniques - Parameter extraction methods and test structures - High-frequency measurement, calibration and de-embedding techniques - RF and thermal simulation techniques - Modelling of passives, interconnect and packages - Statistical modelling - Device, process and circuit simulation - CAD/modelling of power devices - Packaging of power devices.

PROCESS AND DEVICE TECHNOLOGY
Device and IC manufacturing processes, testing methodologies, & reliability - Integration of III-V devices on Si - High performance devices such as GaN power conversion devices - near-THz SiGe HBTs & InP HEMTs - Novel devices such as tunnel FETs (TFETs) - carbon nanotubes, MEMS, graphene & diamond transistors. Optoelectronic and photonic devices such as optical modulators, lasers, photodetectors, and Silicon Photonics - Thermal management technologies, thermal simulation - Advanced packaging of high-power devices and ICs. Advances in processes and device structures demonstrating high speed, low power, low noise, high current, high voltage, etc. BiCMOS processes - Advanced process techniques - Si and SiC homojunction bipolar/BiCMOS devices and SiGe heterojunction bipolar/BiCMOS devices - Manufacturing solutions related to Bipolar and BiCMOS yield improvements - Fabrication of high-performance passive components, sensors, and MEMs - Process technology related to discrete and integrated bipolar/BiCMOS power devices - IGBT, RF power devices. Wide bandgap bipolar devices (e.g., SiC) and related process technology - 3D Integration - Reliability and testing for IC manufacturing

IMPORTANT DATES
Friday May 3, 2019 – Abstracts Due
Friday, June 21, 2019 – Decision E-mail Sent
Friday, August 30, 2019 – Final Manuscript Due

Authors must submit an abstract (not more than 4 pages including figures and other supporting material) of results not previously published or not already accepted by another conference. Papers will be selected on the basis of the abstract.
The abstract must concisely and clearly state:

a) The purpose of the work
b) What specific new results have been obtained
c) How it advances the state-of-the-art or the industry
d) References to prior state-of-the-art
e) Sub-committee preference:
   - Analog, RF, and Microwave ICs
   - Device Physics
   - High-Speed Digital, Mixed-Signal, & Optoelectronic ICs
   - Modeling & Simulation
   - mm-Wave and THz ICs
   - Process & Device Technology

Abstracts must include: title, author(s) name(s) and affiliation(s), corresponding authors' postal and e-mail addresses, and telephone numbers. The committee will honor the authors' committee preference but reserves the right to review the paper in other categories.

Company and governmental clearances must be obtained prior to submission of the abstract.

Accepted work may be used for publicity purposes. Portions of the abstracts may be quoted in articles publicizing the Symposium. Please note on the abstract if this is not acceptable.

Abstracts (PDF only) must be submitted electronically.

Authors will be informed of a decision by June 21, 2019. Authors of accepted papers are required to submit a 4-page camera-ready PDF by August 30, 2019 for inclusion in the Symposium Digest.

Further questions on abstract submission may be addressed to the Symposium Technical Program Co-Chairs:

Bruce Green	The' Linh Nguyen
NXP	Finisar
Ph: +1 480-413-4620	Ph: +1 408-9548-1000
bruce.green@nxp.com	thelinh.nguyen@finisar.com

Symposium information, including abstract submission instructions and a link to the abstract submission system is available on the BCICTS website at: http://www.bcicts.org

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