

A Brief History of GaAs Technology at the GaAs IC Symposium and the Compound Semiconductor IC Symposium

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Over the last four decades, the IEEE Compound Semiconductor IC Symposium (CSICS), formerly the Gallium Arsenide Integrated Circuits (GaAs IC) Symposium, has brought III-V device and microwave circuit engineers and researchers together in a stimulating, highly engaging environment. This column gives some background on GaAs IC Symposium, later renamed the Compound Semiconductor Symposium (CSICS) as shown in the timeline history of Figure 1. It recounts the early history of GaAs technology advancements reported on at the symposium as well as the evolution to CSICS.

In the mid 1970's GaAs RF technology was based on Microwave Integrated Circuits (MIC's). These were not IC's in the sense we know them today because they were made using discrete active and passives components assembled on ceramic substrates. The commercial GaAs chips were manufactured by the large electronic Japanese conglomerates and a few small U.S. companies. A few forward thinking R&D teams in the U.S. were pursuing GaAs digital IC's through government contracts. The GaAs IC Symposium was initiated to provide a public forum for this new digital IC technology based on GaAs. Some of these early pioneers were convinced that in time GaAs IC's would displace Si IC's and become the workhorse of digital technology.

The first GaAs IC Symposium was held in 1979 in Lake Tahoe, California with between 100 and 200 attendees. In the early years, the symposium digest was more like a pamphlet with single page abstracts for each paper. The technical committee reviewed all submitted papers, but the acceptance criteria were very loose. Once, a very well respected committee member proposed that any paper showing a reasonable device I-V characteristic on a curve tracer be accepted so that the technical community could hear how the device was fabricated. The symposium developed the reputation as the place to report the latest GaAs IC developments.

A Journey Through GaAs History at the GaAs IC Symposium

Virtually all of the early advances in GaAs technology were reported at this symposium and a lot of advancements were needed. At this time, GaAs wafers were not round, but rather D-shaped because the ingots were grown in a horizontal boat. If you needed to check something about how the device fabrication was proceeding you did not hesitate to break off a small piece of the wafer for analysis. The brittleness of GaAs made this very easy. Some of the early advances in GaAs technology are reviewed in the next several paragraphs.

A truly digital technology could not depend on the reproducibility and uniformity of epitaxial growth and therefore an ion implantation technology was needed. This was a major issue because, when heated, GaAs starts outgassing arsenic at about 400°C. This was clearly evident by the arsenic oxides (white powder) seen at the exhaust port of ohmic contact annealing furnaces. Therefore a cap which would stand up to the ion implantation anneal temperature was needed. In the beginning each R&D group had their own cap recipe that included a wafer clean and deposition of a silicon nitride and/or silicon oxide cap.

Even if you had a cap that would not delaminate during annealing some of the semi-insulating GaAs wafers could lose their semi-insulating property during annealing. This semi-insulating property significantly reduced substrate capacitance and therefore was essential for the high speed of GaAs digital IC's. At the time semi-insulating GaAs wafers were doped with Cr to create deep levels that trapped electrons giving them this important property. After GaAs ingots were grown crystal growers would supply sample wafers to a potential buyer who would then try to qualify the Cr doped substrate with their own proprietary capping process. If the sample wafer passed, the customer would then purchase the other wafers from the same ingot in hopes that all

the remaining wafers would work in their IC process. If a customer rejected a particular ingot the wafer supplier would not hesitate to send a sample wafer from that same ingot to other customers in hopes that the ingot could be qualified in a different anneal process. This was accepted practice at the time.

Charles Evans provided the first insight into why some wafers did not retain their semi-insulating property during annealing. The intentionally doped Cr was being depleted from the wafer surface during annealing even though the implant cap remained intact. GaAs wafers had to remain semi-insulating following the cap and anneal process in order to be suitable for digital IC's. At some point, boat-grown D-shaped GaAs wafers were replaced by round wafers grown by other processes and other means were found to produce semi-insulating substrates without Cr doping.

Because the GaAs ohmic metal stack was gold-based, all of the other metallization was also gold-based. This required that the metal layers be formed using liftoff. At times this process was very problematic by not working as planned. Soaking the wafer in acetone for hours just did not help. One solution was to soak the exposed photoresist in chlorobenzene which hardened the top layer. This produced an opening in the resist with a retrograde profile making the liftoff process more reproducible and increased device yield. This process was reported at the symposium.

Marty Lepselter was a well respected Bell Labs researcher who, among other things, pioneered e-beam lithography. He was quoted in a news release that short gate length Si would "blow GaAs out of the water". This comment led to a debate at the 1981 GaAs IC Symposium in San Diego. Marty's hypothesis was that short gate length Si digital IC's would out-perform GaAs IC's overcoming GaAs higher electron mobility and low capacitance, semi-insulating substrate. Of course each side believed that they had won the debate, but as we have seen, Marty was right about short gate length Si. The advent of the stepper pushed e-beam lithography aside because of its higher wafer throughput.

Back-gating was another phenomena reported at the symposium. The semi-insulating property of GaAs was not sufficient to perfectly isolate one digital device from a neighboring device. An isolated nearby ohmic contact could act as a parasitic gate electrode through the substrate. This could be seen on a curve tracer by connecting the parasitic gate pad to the gate electrode of the curve tracer. The saturated drain current could be modulated and a small transconductance could be measured.

In addition to the technology problems that had to be solved, the GaAs digital gate that used depletion mode FET's had the added problem of needing to have an output level shifting device. This required that a GaAs digital gate had to have more devices than the equivalent digital gate in Si MOSFET technology. These extra devices in the gate impeded the drive to higher density GaAs IC's.

In the early 1980's, Fujitsu announced the first AlGaAs/GaAs heterojunction transistor. It is interesting that Bell Labs invented the heterojunction concept, but Fujitsu was the first to report a functioning device. These early HFET's would often have drifting DC characteristics as seen on a curve tracer. However, as we know, this problem was also solved and, along with many others, was reported at the GaAs IC Symposium. The success of these advancements was often demonstrated with ring oscillators. When asked about the yield of his ring oscillators, the researcher responded that his circuit yield was sufficient to meet the worldwide demand for ring oscillators.

The last gasp for GaAs digital technology occurred in the late 1990's with the demonstration of a self-aligned, complementary, heterojunction GaAs technology (CGaAsTM). Even though several nearly 1 GHz VLSI circuits were demonstrated, investment in GaAs digital technology was reduced in the face of rapidly advancing Si CMOS, BiCMOS, and SiGe technologies that offered larger wafer size, lower cost, finer line lithography, and abundant resources.

Attendance at the GaAs IC Symposium swelled to more than 900 attendees in the mid 1980's as U.S. government funding floodgates for GaAs MMIC technology opened and many researchers rushed into the GaAs IC arena. It was also during this time that the advances in device technology discussed previously led to state-

of-the-art GaAs MMIC's. Also, new III-V technologies such as InP-based HEMT devices began to mature and show state-of-the-art performance.

During the early and mid 1990's, researchers began to present papers on new technologies such as GaAs HBT's and SiC and GaN wide bandgap semiconductors at the GaAs IC Symposium. As with GaAs device technology, these new devices had similar issues that had to be solved. The late 1990's also saw the rise of SiGe HBT technology. Also at the same time, as GaAs HEMT and MESFET technologies matured, high volume applications such as handset PA's became frequent topics at the GaAs IC Symposium. Like the debates over whether Si or GaAs would dominate high speed digital devices more than a decade earlier, debates over whether SiGe HBT's or GaAs technology would dominate microwave PA applications also figured prominently at the GaAs IC Symposium from 1998 to 2000.

During the early 2000's, new high speed and high power technologies such as GaN, InP, and SiGe became more mainstream and more frequent topics at the symposium. To reflect this, in 2004, the name of the symposium was changed from the GaAs IC Symposium to the Compound Semiconductor IC Symposium (CSICS). With its new name, CSICS continued the GaAs IC Symposium legacy of top quality papers in a congenial atmosphere.

In the 2010's, CSICS covered state of the art microwave/mm-wave devices, IC's, and power amplifiers (PA's) in GaAs, GaN, InP, SiGe, and CMOS technologies. State-of-art device technologies were presented for ultra-high speed as well as ultra-high power applications. Emerging areas such as silicon photonics became a part of the symposium as well. Over the years, GaAs IC and CSICS have hosted papers with state of the art MMIC PA power & efficiency, sample & hold circuit speed, mm-wave IC power, gigabit IC performance, frequency divider operating frequency, and many other state-of-the-art benchmarks.

In 2018 BCTM and CSICS are merging into one symposium: BCICTS

Starting in 2018, the IEEE Bipolar and BiCMOS Circuits and Technology Meeting (BCTM) and the IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) will join forces and merge under a new name: IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) pronounced pronounced "Be-Six." After 39 years of the Compound Semiconductor IC Symposium (CSICS), and 32 years of the Bipolar/BiCMOS Circuit and Technology Meeting (BCTM), this new combined symposium will be held on Sunday October 14 to Wednesday October 17, 2018 in San Diego, California.

Both BCTM and CSICS bring a long history as international gatherings where distinguished experts present their latest results in bipolar, SiGe BiCMOS, and compound semiconductor circuits, devices, and technology. There are no other events in the world where you can see leading edge Bipolar/BiCMOS devices and technology, 5G ICs, GaN HPAs, InP THz PAs, optical CMOS/SiGe transceivers, GaN HEMT power devices, and advances in compact modeling all presented together. Additional information about BCICTS can be found on the BCICTS website, <http://www.bcicts.org/>.

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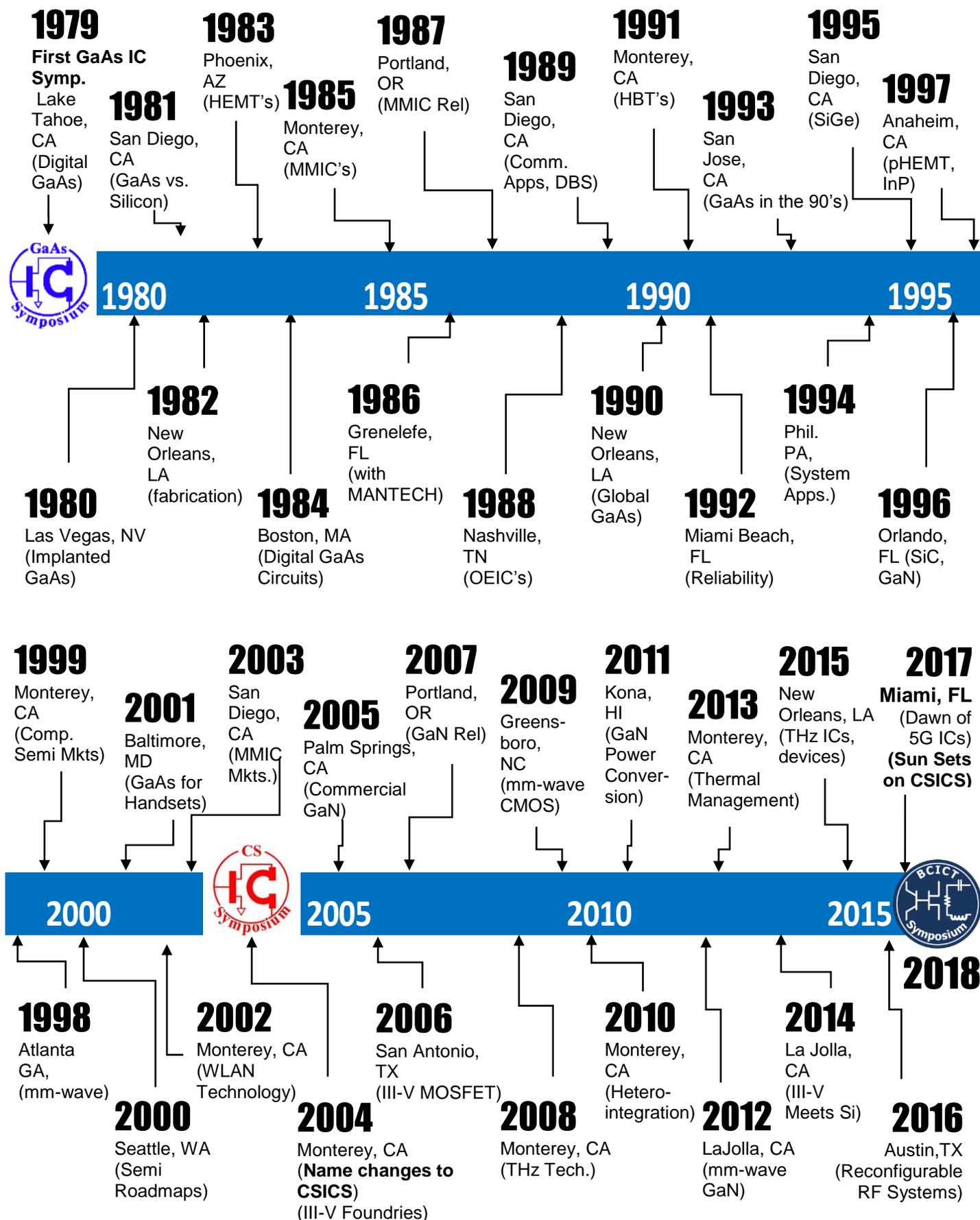


Figure 1: GaAs IC and CSIC Symposium history at a glance with “hot topics” in parentheses.



Figure 2: The sun sets (literally!) for CSICS 2017 in Miami as several TPC and Excom members enjoy an informal gathering after the conference.