ADVANCE PROGRAM

BCICTS 2022
IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium

October 16-19, 2022

SPONSORED BY

THE ELECTRON DEVICES SOCIETY OF THE INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS

IN COOPERATION WITH

THE IEEE SOLID - STATE CIRCUITS SOCIETY
THE IEEE MICROWAVE THEORY & TECHNIQUES SOCIETY

Conference Website: https://bcicts.org

2022 BCICTS Schedule at a Glance

Sunday – October 16	
SHORT COURSE Millimeter-wave and THz applications – Systems, circuits, devices and technologies **Valley of the Sun Ballroom AB**	
7:30AM 5:00PM	Registration for Short Course Only **Valley of the Sun Ballroom Foyer**
8:00AM 8:45AM	Breakfast Short Course & Primer **Valley of the Sun Ballroom Foyer**
8:45AM 8:50AM	Welcome & Speaker Introduction, M Schroter, TU Dresden **Valley of the Sun Ballroom AB**
8:50AM 9:50AM	Millimeter-wave sensing – circuits, systems and applications Part 1, A. Paidimarri, IBM **Valley of the Sun Ballroom AB**
9:50AM 10:00AM	Coffee Break for Short Course Only **Valley of the Sun Ballroom Foyer**
10:00AM 11:00AM	Millimeter-wave sensing – circuits, systems and applications Part 2, A. Paidimarri, IBM **Valley of the Sun Ballroom AB**
11:00AM 11:10AM	Coffee Break for Short Course Only **Valley of the Sun Ballroom Foyer**
11:10AM 12:10PM	Circuit Design for Millimeter-wave applications in communication and sensing – Part 1, J. Long, U.Waterloo **Valley of the Sun Ballroom AB**
12:10PM 1:10PM	Lunch Break for Short Course Only **Oculus Terrace 2nd floor**
1:10PM 2:10PM	Circuit Design for Millimeter-wave applications in communication and sensing – Part 2, J. Long, U.Waterloo **Valley of the Sun Ballroom AB**
2:10PM 2:20PM	Coffee Break for Short Course Only **Valley of the Sun Ballroom Foyer**
2:20PM 3:20PM	SiGe BiCMOS technology for mm-wave and THz applications, P. Chevalier, ST ***Valley of the Sun Ballroom AB***
3:20PM 3:30PM	Coffee Break for Short Course Only **Valley of the Sun Ballroom Foyer**
3:30PM 4:30PM	InP technology for mm-wave and THz applications, M. Urteaga, Teledyne **Valley of the Sun Ballroom AB**
4:30PM 4:45PM	Adjourn and feedback
PRIMER Simulation methods and tools for RF design **Valley of the Sun Ballroom D**	
7:30AM 12:50PM	Registration for Primer Only **Valley of the Sun Ballroom Foyer**
8:00AM 8:45AM	Breakfast for Primer Only **Valley of the Sun Ballroom Foyer**
8:45AM 8:50AM	Welcome & Speaker Introduction, D. Weiser, TI **Valley of the Sun Ballroom D**
8:50AM 11:00AM	Simulation methods and tools for RF design Part 1, K. Gullapalli, NXP **Valley of the Sun Ballroom D**
11:00AM 11:10AM	Coffee Break for Primer Only **Valley of the Sun Ballroom Foyer**
11:10AM 12:40PM	Simulation methods and tools for RF design Part 2, K. Gullapalli, NXP **Valley of the Sun Ballroom D**
12:40PM 12:50PM	Adjourn and feedback

Monday – October 17

8:00AM 5:00PM	Registration **Valley of the Sun Ballroom Foyer**	
9:00AM 9:30AM	Welcome and Announcements **Valley of the Sun Ballroom AB**	
9:30AM 10:10AM	Plenary Session 1 **Valley of the Sun Ballroom AB**	
10:10AM 10:40AM	Coffee Break	
10:40AM 11:20AM	Plenary Session 2 **Valley of the Sun Ballroom AB**	
11:20AM 12:00PM	Plenary Session 3 **Valley of the Sun Ballroom AB**	
12:00PM 1:30PM	Lunch Break **Self-Arrangement**	
1:30PM 3:10PM	**1a.** High Performance Devices in InP and GaN **Valley of the Sun AB**	**1b.** Amplifier and Transceiver Techniques for >100 GHz Operation (1:50PM) **Valley of the Sun DE**
3:10PM 3:40PM	Coffee Break	
3:40PM 5:00PM	**2a.** Reliability, Dynamic modeling, TCAD extraction with Neural Networks **Valley of the Sun AB**	**2b.** mmW & THz Signal Generation **Valley of the Sun DE**
5:00PM 7:30PM	Exhibition Reception **Valley of the Sun Ballroom C**	

Tuesday – October 18

8:00AM 5:00PM	Registration **Valley of the Sun Ballroom Foyer**	
8:30AM 9:30AM	Exhibition Breakfast **Valley of the Sun Ballroom C**	
9:40AM 11:00AM	**3a.** Modeling of Scaling and Distributed Effects in III-V Devices **Valley of the Sun AB**	**3b.** SiGe Technology (10:00AM) **Valley of the Sun DE**
11:00AM 11:30AM	Coffee Break **Valley of the Sun C**	
11:30AM 12:30PM	**4a.** Electrothermal modeling and parameter extraction of SiGe HBTs **Valley of the Sun AB**	**4b.** III-V Amplifiers **Valley of the Sun DE**
12:30PM 2:00PM	Exhibition Lunch **Valley of the Sun Ballroom C**	
2:00PM 3:40PM	**5a.** Advancements in GaN HEMT Modeling and Simulations **Valley of the Sun AB**	**5b.** III-V mmW Power Amplifier Technologies **Valley of the Sun DE**
3:40PM 4:10PM	Coffee Break **Valley of the Sun Ballroom C**	
4:10PM 5:30PM	**6a.** Bipolar Device Physics **Valley of the Sun AB**	**6b.** III-V Amplifiers **Valley of the Sun DE**

Wednesday – October 19

7:30AM 5:30PM	Registration **Valley of the Sun Ballroom Foyer**	
8:30AM 10:10AM	**7a.** High Frequency GaN and UWBG Devices **Valley of the Sun AB**	**7b.** Advancements in SiGe Circuit Designs (8:50AM) **Valley of the Sun DE**
10:10AM 10:40AM	Coffee Break **Valley of the Sun Foyer**	
10:40AM 11:40AM	**8a.** Late News 1 **Valley of the Sun AB**	**8b.** Late News 2 **Valley of the Sun DE**
11:40AM 12:45PM	Closing Reception **Valley of the Sun Ballroom Foyer**	
12:45PM 1:00PM	Closing Session **Valley of the Sun AB**	

Welcome from the BCICTS 2022 Chairs

It is with great pleasure that we welcome you to participate in the 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS). After 43 years of the Compound Semiconductor IC Symposium (CSICS), and 36 years of the Bipolar/BiCMOS Circuit and Technology Meeting (BCTM), the fifth meeting of this combined symposium will be held in person from Sunday October 16 to Wednesday October 19 at the Sheraton Phoenix Downtown, in Phoenix Arizona.

The planning committee looks forward with great anticipation at this opportunity to return to meeting in person, after holding the past two BCICTS conferences virtually due to the COVID-19 pandemic. This a great opportunity for us in the engineering and technical community to reconnect with each other both professionally and personally, to meet new colleagues and visit with long-time friends, while catching up on the latest trends within microelectronics.

This year, BCICTS will continue the long history, from BCTM and CSICS, of international symposiums where distinguished experts present their latest results in bipolar, SiGe BiCMOS, and compound semiconductor circuits, devices, and technology. There are no other events in the world where you can see leading edge bipolar/BiCMOS devices and technology, 5G ICs, GaN HPAs and RF switches, InP THz PAs, optical CMOS/SiGe transceivers, and advances in compact modeling, all presented together.

This fifth BCICTS includes presentations from worldwide submissions on all aspects of the technology. Sessions will span the range from the latest research developing high performance GaN and InP RF devices as well as SiGe optical receivers. There are sessions exploring the latest mmW and THz circuits and their performance, in combination with sessions on characterizing, modeling and simulating these new technologies. The Plenary talks the BCICTS program committee has arranged this year reflects this breadth of topics, with distinguished technical leaders covering topic on devices, circuits and modeling: the innovative RF devices needed for next generation communications (Kozo Makiyama, Sumitomo Electric Industries); High-performance design and components needed for optical electronics (Kodaba Lakshmikumar, Cisco Systems); and device modeling tools and their application to SiGe HBT development (Michael Schröter, TU Dresden).

This year as we have done in past years, BCICTS will offers a topical short course and a more basic primer course. Both will be taught by leading experts, with the short course intended for professionals seeking comprehensive understanding of the latest industry trends and techniques, and the primer as an introductory tutorial. The short course topic this year is “Millimeter-wave and THz applictions – Systems, circuit devices and technologies, and will cover mmW sensing, circuit design for mmW applications in communication, as well as both SiGe BiCMOS and InP technologies for mmW and THz applications. The primer topic this year will be “Simulation methods and tools for RF design”.

We would like to thank the many dedicated volunteers on the BCICTS Committee, and the generous support of the IEEE Electron Devices, Microwave Theory and Techniques, and Solid-State Circuits Societies. Finally, we look forward to interacting with all participants to continue the traditions of technical excellence for BCICTS!

Robert Howell, Symposium Chair
Northrop Grumman
Craig Steinbeiser, Symposium Co-Chair
Qorvo

BCICTS 2022 REGISTRATION

Click here to register https://bcicts.org
Advance registration deadline is Monday, August 15, 2022.

Please note: Registration is required for all attendees including SESSION CHAIRS and PRESENTERS. Only paid attendees will be admitted to the workshops, technical sessions, and exhibition hall.

The following steps will guide you through the registration process:

Membership
To receive IEEE member rates, you will enter your IEEE login within the registration system for an immediate automatic lookup. If you are not an IEEE member and would like to learn about the advantages of being a member and receiving the conference member rate, please visit www.ieee.org/services/join or call 1-800-678-IEEE. Please note that you must be a member at the time of registration to receive the member rate.

Hotel Confirmation #
Please be sure to reserve your hotel room prior to completing your registration. Your confirmation # will be required to complete your registration. You can reserve your room using the link below:

Refund/Cancellation Policy:
All requests for refund/cancellation must be received in writing at least 15 days prior to the conference start date. Any requests thereafter will not be entitled to a refund. Cancellations will incur a $50 USD administration fee. Please submit cancellation requests via email (cs@cshawevents).

BCICTS 2022 REGISTRATION FEES

***Request Hotel confirm code with 7 digits**

	ADVANCE Registration Before September 15th	Late Registration after September 15th	Registration without Hotel
IEEE Members	$825	$925	$1,125
Non-Members	$990	$1,090	$1,290
Student	$425	$525	$720
Student Non-Member	$504	$550	$750

Registration Fees: SHORT COURSE **Sunday, October 16 from 8:30 am to 5 pm**

(1) Course Cost (includes course materials both electronic and hard copy, breakfast, lunch, and breaks):

Type	Registration	Late Registration after September 15th
IEEE Member	$500	$600
Non-Members	$720	$820
Student	$350	$450
Student Non-Member	$420	$520

Registration Fees: PRIMER COURSE **Sunday, October 16 from 8:30 am to 12:30 pm**

(1) Course Cost (includes breakfast and BREAKS):

TYPE	Registration	Late Registration after September 15th
IEEE Member	$415	$515
Non Member	$498	$598
Student	$300	$400
Student Non-Member	$360	$460

HOTEL RESERVATIONS

A block of rooms has been reserved at special discounted rates for BCICTS conference participants at our host hotel below. While there are alternatives, we would like to remind attendees to please support the conference and fully enjoy all the activities by staying at the official host hotel. The symposium relies on attendees staying at the conference hotel. Room reservations should be made as soon as possible before the hotel cut-off date below, as there are a limited number available at the group rate.

Booking Website:
https://book.passkey.com/e/50273940

Check-in Time: 3:00 pm
Check-out Time: 12:00 noon
Group rates: **$229.00** per night

Next Step: Register Here: https://cvent.me/YdEOmq

Additional Hotel Fees (For those staying outside of the discounted hotel block)
This year, to help ensure financial success, we are implementing an added registration charge for individuals that opt to stay outside of our discounted group hotel block. We apologize for any inconvenience this may cause and appreciate your efforts to stay at our host hotel.

Questions and Issues: If you have additional questions or need assistance, please contact, **Catherine Shaw, CMP, BCICTS Conference Director** at cs@cshawevents.com.

Travel

Air Travel

- Phoenix Sky Harbor International Airport is located 3.8 miles from the hotel.
- Visit airport website: https://www.skyharbor.com
- Alternate Airport Transportation: https://www.execucar.com/
- Or take a taxi upon arrival using designated taxicab stations upon arrival

Parking:

Parking is available on property.
On-Site Parking:

- Daily: $26
- Weekly: $161
- Valet Daily: $36

Things to Do in Phoenix:

Click below to view some fun things to do during your stay in Phoenix:

Visit Phoenix: https://www.visitphoenix.com
Tour information: https://www.viator.com/Phoenix/d639 *Not included within conference registration fees.
Top Roof Tops and Bars in Phoenix: https://www.visitphoenix.com/stories/post/rooftop-bars/
Top Restaurants in Phoenix:
https://www.thrillist.com/eat/phoenix/best-restaurants-phoenix
https://www.tripadvisor.com/Restaurants-g31310-Phoenix_Arizona.html

Visit Phoenix Deals:
Phoenix Deals features local restaurants and attractions specifically for meeting attendees. The link below is 100% browser based and does not require downloading an app or printing coupons. Access this link to save money while still experiencing the destination: https://explore.visitphoenix.com/checkout/261/visit-phoenix/1472/visit-phoenix-downtown-deals

Digital Swag
Enjoy this collection of downloadable Phoenix inspiration including wallpapers, gifs, frames, digital jigsaw puzzles and Spotify playlists!
https://www.visitphoenix.com/digital-swag/

We look forward to seeing you in Phoenix. If you should have questions or need assistance during the planning process, please send a message to the specific contact below.

Catherine Shaw
BCICTS Conference Manager
cs@cshawevents.com

On-site Conference Registration Desk Hours:

Registration will be open in the Main Valley of the Sun Ballroom Ballroom # C right outside of the Ballroom – 2nd floor.

Sunday,	October 16	7:30 AM - 5:00 PM
Monday,	October 17	7:30 AM - 5:00 PM
Tuesday,	October 18	7:30 AM - 5:00 PM
Wednesday,	October 19	7:30 AM - 5:00 PM

Conference Networking & Social Events:

Several networking events have been arranged to promote informal social interactions among conference participants. Event details are listed below for your reference:

Monday, October 17: Exhibitor Reception from 5:00 PM to 7:30 PM; Location: Valley of the Sun Ballroom C

Tuesday, October 18: Exhibitor Breakfast from 8:30 am to 9:30 am

Tuesday, October 18: Conference Exhibitor luncheon from 12:30 pm to 2:00 pm

Wednesday, October 19: Conference Closing reception – Valley of the Sun Ballroom Foyer or Oculus Terrace (Weather permitting) 11:50 am to 12:45 pm

Attendee Lounge & Speaker Ready Room:
The Attendee Lounge/Speaker Ready Room will be available inside the Valley of the Sun Ballroom C from 8:00 AM - 5:00 PM daily.

ADDITIONAL INFORMATION

ADMISSION All interested persons are welcome to register and attend the BCICTS; you do not have to be an IEEE member. Admission to sessions requires a BCICTS badge. Please wear your badge at all times.

REGISTRATION Complete registration information is contained in the centerfold of this booklet as well as on the conference's web page (https://bcicts.org) Please use the website to register. The advanced registration deadline is **September 15**. All conference activities are included in the registration fees (technical sessions, food breaks and the banquet) as well as a USB flash drive with an electronic copy of BCICTS 2022 Proceedings.

OTHER CONFERENCE SOCIAL EVENTS Several events have been arranged to promote informal social interactions among conference participants.

TUTORIAL / SURVEY TALKS Tutorial talks given by invited experts are intended to give a broad overview of a given subject with a critical review of technology and applications. They are twice the length of the usual contributed talk with longer abstracts in the Proceedings.

MEMBERS OF THE PRESS: You are welcome to attend BCICTS. Admission is free. Just present your business card at the registration desk.

RECRUITING Intensive recruiting undermines the purposes for which the BCICTS was established, and is contrary to IEEE policy.

BEST STUDENT PAPER AND BEST PAPER AWARDS BCICTS offers a Best Paper Award. The BCICTS Best Paper Award recognizes and promotes high quality contributions to scholarly research among professionals who author and present papers at the conference. All papers submitted in non-student category are eligible for consideration for the Best Paper Award.

The BCICTS Best Student Paper Award recognizes and promotes outstanding research led by students. To be eligible for consideration for the Best Student Paper Award, the following criteria have to be met: 1) the student must have carried out a substantial part of the research reported in the paper, 2) the student must be the first author and must present the paper at the conference, 3) the paper must be identified as a student paper during submission of the paper; and 4) the paper identified as a student paper in submission, but not presented by the student will be disqualified for Best Student Paper Award competition. In this scenario, the paper will be moved to non - student category for Best Paper Award competition automatically.

Eligible papers are evaluated by the Best Paper Award Committee and the notifications will be sent out after the conference. The winners of the awards will be recognized with a $500 check and a plaque at next year's BCICTS conference.

FURTHER INFORMATION BCICTS is sponsored by the IEEE Electron Devices Society (EDS) in co - operation with the IEEE Solid - State Circuits Society (SSCS) and the IEEE Microwave Theory & Techniques Society (MTT).

BCICTS 2022 Short Course

Valley of the Sun Ballroom AB

Date: Sunday, October 16, 2022
Time: 8:00 AM – 4:45 PM
Topic: Millimeter-wave and THz applications – Systems, Circuits, Devices and Technologies

Speakers:

- Arun Paidimarri (IBM)
- John R. Long (University of Waterloo)
- Pascal Chevalier (STMicroelectronics)
- Miguel Urteaga (Teledyne)

8:00 – 8:45 AM **Registration and breakfast**
8:45 – 8:50 AM **Welcome**
Michael Schroter (TU Dresden)

8:50 – 9:50 AM
Millimeter-wave sensing – circuits, systems and applications, Part 1
Instructor: Dr. Arun Paidimarri, IBM T.J. Watson Research Center, USA

Abstract: The development and progression of phased array systems for communications and sensing has accelerated with mmWave 5G. High-performance phased arrays have been demonstrated at frequencies up to 60-GHz with research prototypes going all the way up to 300GHz. These devices promise to enable new sensing applications co-existing with communications in the context of 6G systems. In this talk, we present phased array architectures and examples of how they are integrated at the system level to enable sensing applications. We also present digital control architectures that are necessary to orchestrate the sensing in concert with the baseband signals. We then present three example applications of sensing using some of the phased array systems developed at IBM Research.

We describe a high-speed 3D radar data acquisition system operating at 60GHz with a16-element phased array. It is engineered to acquire 100s of frames per second using 1 GHz of bandwidth and scanning across 441 directions. An AI algorithm is then trained to automatically recognize events using the 3D radar data. Two use cases are presented: (1) hand gestures classification, and (2) classification of concealed objects in motion.

We demonstrate a multi-spectral imaging platform "hyperimager" consisting of sensors, an App, and cloud infrastructure. The sensors include the 3D radar system at 60GHz, IR and visible-domain information. The system is able to capture multi-spectral images that can exploit the advantages of each domain. We also demonstrate a joint communications and 3D sensing application using IBM's Software Defined Phased Array Radio (SDPAR). The SDPAR uses a state-of-the-art 28GHz 64-element phased array in conjunction with a SDR and a common API to ease system development of applications using phased arrays. 3D sensing is obtained by time-of-flight measurement using OFDM waveforms that are already in use for communications. A total of 1GHz of sensing bandwidth is obtained by stitching 100MHz wide packets across time. Such a joint sensing-communication doesn't affect underlying communication bandwidth.

We finally present a scalable, Software-Defined, Platform for <6-GHz and 28-GHz RF data collection, storage, and analysis. The system enables high-speed ingestion of I/Q data streams, large storage and APIs to easily consume and analyze data, and compute architecture for running algorithms including AI/ML. The system could thus be utilized for running many of system ideas described in this talk and provides a platform for developing many more in the future.

Arun Paidimarri received the B.Tech degree in electrical engineering from the Indian Institute of Technology, Bombay, India, in 2009 and the S.M. and Ph.D degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA in 2011 and 2015 respectively. He is currently a Research Staff Member at the IBM T.J. Watson Research Center, Yorktown Heights, NY. His research interests are in low power wireless system design, mm-wave circuit design and software-defined phased arrays. He is a member of the technical program committees for RFIC Symposium and BCICTS. Dr. Paidimarri is a co-recipient of the best-paper awards at the IEEE International Conference on Communications (ICC) 2013 and at SmartCom 2019. He was awarded the President of India Gold Medal in 2009. He won a Silver Medal at the 37th International Chemistry Olympiad held in Taipei, Taiwan in 2005.

9:50 – 10:00 AM Break

10:00 – 11:00 AM
Millimeter-wave sensing – circuits, systems and applications, Part 2
Instructor: Dr. Arun Paidimarri, IBM T.J. Watson Research Center

11:00 – 11:10 AM Break

11:10 – 12:10 AM
Circuit Design for Millimeter-wave applications in communication and sensing, Part 1
Instructor: Prof. John R. Long, University of Waterloo, Canada

Abstract: Millimeter-wave front-end circuits employed in communication and sensing applications are described in this lecture. Typical circuit blocks and their design are presented and analyzed. These include: low-noise amplifiers (LNAs), T/R switches, phase shifters, voltage-controlled oscillators (VCOs and DCOs), frequency multipliers, mixers, and power amplifiers (PAs). The performance of lumped-element varactors, inductors, and transformers integrated on-chip and used in the design and optimization of these circuits is also reviewed. Scaling and modeling of on-chip passives for application in VCO/DCO resonators, low-loss feedback networks, baluns, power combiners/splitters, biasing and peaking networks are discussed. Circuit impairments caused by physical layout and back-end technology constraints at mm-wave frequencies are highlighted. Finally, substrate shielding methods, which is essential to reduce substrate losses (esp. for silicon) at mm-wave frequencies, are also described.

John R. Long received the B.Sc. from the University of Calgary in 1984, and the M.Eng. and Ph.D. degrees in Electronics Engineering from Carleton University in Canada in 1992 and 1996, respectively. He has worked at Bell-Northern Research Ltd. (Ottawa), the University of Toronto (1996-2001), and the Delft University of Technology in the Netherlands (2002-2014). In January 2015, he joined the ECE Department at the University of Waterloo in Canada. His current research interests include low-power transceiver circuitry for highly integrated radio and high-speed data communication applications. He is an IEEE Fellow and is currently president of the IEEE Solid-State Circuits Society.

12:10 – 1:10 PM Lunch

1:10 – 2:10 PM
Circuit Design for Millimeter-wave applications in communication and sensing, Part 2
Instructor: Prof. John R. Long, University of Waterloo, Canada

2:10 – 2:20 PM Break

2:20 – 3:20 PM

SiGe BiCMOS technology for mm-wave and THz applications

Instructor: Dr. Pascal Chevalier, STMicroelectronics, France

Abstract: SiGe BiCMOS technology enjoys a continuous improvement of Silicon Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) performance combined nowadays with nanoscale CMOS nodes (90nm an below). It allowed accompanying the Ethernet communication roadmap (from few Gb/s to several hundred of Gb/s today) and serving millimeter-wave applications for wireless infrastructures and automotive radars. Today we are discussing the use of SiGe for the 6th generation of mobile communication, including at sub-THz frequencies.
This lecture will start with a review of the figures of merits, assets and state-of-the-art of SiGe BiCMOS, and its positioning versus other competing technologies. Vertical and lateral scaling principles and the related trade-offs driving the choice of the SiGe HBT device architecture will be presented after a reminder on device physics basics. Next, performance of CMOS and passive devices will be exhibited along with the related integration challenges using STMicroelectronics' technologies example.
Finally, the capability of SiGe BiCMOS to address THz applications will be discussed. It will be shown that a low-cost transceiver enabling a 100 Gb/s link at 150 GHz can be fabricated in a 55-nm SiGe BiCMOS technology. Perspectives to address applications above 300 GHz will also be debated in the perspective of the BiCMOS roadmap.

Pascal Chevalier received the Ph.D. degree in electronics from the University of Lille, France, in 1998 for his work on InP-based HEMT. He joined Alcatel Microelectronics, Belgium, in 1999, where he contributed to the start of RF BiCMOS. Since joining STMicroelectronics, Crolles, France, in 2002, he has been working on the development of SiGe BiCMOS and RF-SOI CMOS technologies and related devices, with a long-lasting research interest in SiGe HBT. He is currently leading the RF-SOI CMOS, BiCMOS & Disruptive Technologies R&D team and is a Senior Member of Technical Staff. Dr. Chevalier has authored or co-authored over 200 technical journal papers and conference publications. He has served the Technical Program Committees of the IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM) and the ECS SiGe Symposium. He has been a member of the RF & AMS Technologies section of the ITRS of which he led the Silicon Bipolar & BiCMOS subgroup. He currently serves the Technical Program Committees of the IEEE Bipolar and Compound Semiconductor Integrated Circuits and Technology (BCICTS) and the IEEE International Electron Devices Meeting (IEDM).

3:20 – 3:30 PM Break

3:30 – 4:30 PM

InP technology for mm-wave and THz applications

Instructor: Dr. Miguel Urteaga, Teledyne Scientific Company, USA

Abstract: Future mm-Wave and sub-THz communication systems seek to exploit the large available spectral bandwidth at frequencies >100GHz. Large-element MIMO array architectures envisioned for these systems will require high-performance and high-efficiency frontend elements (power amplifiers, low-noise amplifiers…). Indium phosphide (InP) transistor technologies have demonstrated THz-class device bandwidths. Presently, at frequencies >100GHz, InP-based high electron mobility transistor (HEMT) technologies offer the highest performance low noise amplifiers (LNAs) and InP heterojunction bipolar transistor technologies (HBTs) offer the highest performance power amplifiers (PAs). In this short course, the design and performance of InP HBTs will be reviewed with an emphasis on technology considerations for mm-Wave power amplifier design. InP HBT performance is strongly influenced by non-equilibrium (ballistic) transport effects in the collector and the modeling and impact of these effects on circuit operation will be discussed. Power amplifier results in InP HBT technologies from 100-300GHz will be presented and prospects for improving PA efficiency and output power density will be considered. Finally, techniques that have been demonstrated for the heterogeneous integration of InP technologies with Si technologies will be reviewed.

Miguel Urteaga received his M.S. and Ph.D. degrees in Electrical Engineering from the University of California Santa Barbara in 2001 and 2003, respectively. He is currently the director of Foundry Products and Services for Teledyne Scientific Company and manages the advanced device development group. His research is focused on the development of ultra-high speed transistor technologies, primarily in the InP material system. He has led the development of Teledyne's high performance InP HBT IC technologies. These technologies have been used to demonstrate state-of-the-art integrated circuits ranging from high-speed mixed-signal and digital ICs to mm-wave and THz monolithic integrated circuits. He served as the program manager at Teledyne for the DARPA THz Electronics, Diverse Accessible Heterogeneous Integration (DAHI) and Dynamic Range-enhanced Electronics Materials (DREAM) programs. He has authored or co-authored over 200 conference and journal publications.

4:30 – 4:45 PM Adjourn and feedback

BCICTS 2022 Primer

Valley of the Sun Ballroom D

Date: Sunday, October 16, 2022
Time: 8:00 AM – 12:50 PM
Topic: Simulation methods and tools for RF design

Speaker:

- Kiran K. Gullapalli (NXP)

8:00 – 8:45 AM **Registration and breakfast**
8:45 – 8:50 AM **Welcome**
Doug Weiser (TI)

8:50 – 11:00 AM
Simulation methods and tools for RF design, Part 1
Instructor: Kiran K. Gullapalli, NXP

This primer course was developed to serve as an introductory-level course on simulation methods commonly used in RF and MMW integrated circuit design.
Covered material includes

- Classical circuit simulation principles and requirements for compact models, substrate [and thermal] effects
- Non-linear circuit simulation principles and applications (time, frequency, and mixed frequency-time methods)
- LTI and LPTV small signal analyses and applications
- Modeling distributed structures for circuit simulation (EM simulation)
- Parasitic extraction and reduction
- Examples/Case-studies

Kiran K. Gullapalli received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Madras, Chennai, India, in 1989, and the M.S. and Ph.D. degrees in electrical and computer engineering and the M.B.A. degree from the University of Texas at Austin, Austin, TX, USA, in 1991, 1994, and 2009, respectively.,He joined Circuit Simulation Group, Motorola, Austin, TX, USA, in 1994 and has been working on various aspects of circuit simulation ever since. He worked on Motorola’s in-house circuit simulator, Mica, with a focus on device models and RF simulation. In 2002, he joined Synopsys, Mountain View, CA, USA, where he worked on fast-SPICE techniques. In 2005, he re-joined the Mica Circuit Simulation Group at NXP, Austin, where he continues to work on high performance Analog and RF simulation. In 2017 he was elected NXP fellow for his contributions to Analog and RF simulation.

11:00 – 11:10 AM **Break**

11:10 – 12:40 PM
Simulation methods and tools for RF design, Part 2
Instructor: Kiran K. Gullapalli (NXP)

12:40 – 12:50 PM **Adjourn and feedback**

INTRODUCTORY REMARKS AND PLENARY

WELCOME AND ANNOUNCEMENTS

Monday,9:00 - 9:30 AM – ***Valley of the Sun Ballroom***

Robert Howell, Chair

PLENARY 1

Monday 9:30 AM – ***Valley of the Sun Ballroom AB***
Session Chair: Rob Howell, *Northrop Grumman*
Co-chair: Breandán Ó hAnnaidh, *Analog Devices*

9:30 AM - 10:10 AM - Innovative RF Device Technologies for Advanced Information and Communications Network Society

Kozo Makiyama[1], Shigeki Yoshida[1], Ken Nakata[1], and Yasuyuki Miyamoto[2]
[1] *Sumitomo Electric Industries, Ltd., Yokohama 244-8588, Japan*
[2] *Tokyo Institute of Technology, Tokyo, 152-8552, Japan*

PLENARY 2

Monday 10:40 AM – ***Valley of the Sun Ballroom AB***
Session Chair: Craig Steinbeiser, *Qorvo*
Co-chair: Rob Howell, *Northrop Grumman*

10:40 AM - 11:20 AM - High-Performance CMOS TIA for Data Center Optical Interconnects

Kodaba R. Lakshmikumar[1], Alexander Kurylak[1], Romesh Kumar Nandwana[1], Bibhu Das[1], Joe Pampanin[1], Vito Boccuzzi[1], and Pavan Kumar Hanumolu[2]
[1] *Cisco Systems Inc., Allentown, PA, USA*
[2] *Dept. of Electrical Engineering, University of Illinois at Urbana-Champaign, IL, USA*

PLENARY 3

Monday 11:20 AM – ***Valley of the Sun Ballroom AB***
Session Chair: Breandán Ó hAnnaidh, *Analog Devices*
Co-chair: Craig Steinbeiser, *Qorvo*

11:20 AM - 12:00 PM - Device modeling tools and their application to SiGe HBT development

Michael Schröter, Markus Müller and Mario Krattenmacher
Chair for Electron Devices and Integrated Circuits (CEDIC), TU Dresden, 01062 Germany

Conference Program

1a. High Performance Devices in InP and GaN

Monday 1:30 PM – ***Valley of the Sun Ballroom AB***
Session Chair: Parrish Ralston, *Northrop Grumman*
Co-Chair: Bruce Green, *NXP Semiconductors*

1a.1 (Invited)
1:30-2:10 PM – InP/GaAsSb DHBTs: THz Analog Performance and Record 180-Gb/s 5.5Vppd-Swing PAM-4 DAC-Driver

C.R. Bolognesi[1], A.M. Arabhavi[1], R. Hersent[3], S. Hamzeloui[1], F. Jorge[3], X. Wen[2], M. Riet[3], M. Luisier[2], V. Nodjiadjim[3], F. Ciabattini[1], C. Mismer[3], O. Ostinelli[1], and A. Konczykowska[3,4]
[1] *Millimeter-Wave Electronics Group (MWE), ETH-Zürich, 8092 Zurich, Switzerland*
[2] *Integrated Systems Laboratory (IIS), ETH-Zürich, Switzerland*
[3] *III-V Lab, Nokia Bell Labs, Thales Research and Technology and CEA-LETI, France*
[4] *ADesign, l'Haÿ-les-Roses, France*

1a.2 (Student)
2:10-2:30 PM – Highly-Linear InP/GaAsSb DHBTs with 18.2 dBm OIP3 at 45 GHz: Comparison of Common-Base and Common-Emitter Structures

S. Hamzeloui, F. Ciabattini, A. M. Arabhavi, W. Quan, D. Marti, M. Ebrahimi, O. Ostinelli, and C.R. Bolognesi
Millimeter-Wave Electronics (MWE) Group, ETH-Zürich, 8092 Zurich, Switzerland

1a.3
2:30 -2:50 PM – SLCFET Amplifier Performance Improvements Using an ALD TiN T-Gate Process

Timothy Vasen[1], Brian Novak[1], Marc Scimonelli[1], Kevin Frey[1], Mustapha Saad[1], Abbey Saia[1], Benjamin Grisafe[1], Ken A. Nagamatsu[1], Josephine Chang[1], Virginia Wheeler[2], Karl Hobart[2], Andrew D. Koehler[2], Patrick Shea[1], Stephen Van Campen[1], Robert S. Howell[1], and Shamima Afroz[1]
[1] *Northrop Grumman Mission Systems Linthicum MD 21090*
[2] *US Naval Research Laboratory Washington D.C 20375*

1a.4
2:50 -3:10 PM – Challenges and Potential of N-polar GaN HEMT for beyond 5G Wireless Network

Shigeki Yoshida, Kozo Makiyama, Akihiro Hayasaka, Isao Makabe, and Ken Nakata
Sumitomo Electric Industries, Ltd., Yokohama 244-8588, Japan

1b. Amplifier and Transceiver Techniques for > 100 GHz Operation

Monday 1:50 PM - ***Valley of the Sun Ballroom DE***
Session Chair: Eric Bryerton, *Virginia Diodes, Inc.*
Co-Chair: Marc Rocchi, *OMMIC SAS*

1b.1 (Student)
1:50-2:10 PM – A 1-W/mm2, 140-GHz SiGe HBT Power Amplifier using Optimized Embedding Techniques

Everett O'Malley and James F. Buckwalter
University of California Santa Barbara, Santa Barbara, CA USA

1b.2 (Student)
2:10 2:30 PM – A D-Band Transceiver with On-Chip Multi-Port Radiators and Leakage Cancellation in 45nm SOI
Vincent Lammert[1,2], Michael Leyrer[2], Vadim Issakov[1]
[1] *Institute for CMOS Design, Technical University Braunschweig, Braunschweig, Germany*
[2] *Infineon Technologies AG, Neubiberg, Germany*

1b.3 (Invited)
2:30-3:10 PM – Maximizing Energy Efficiency in Sub-THz Radio Communication and Prospective toward 6G
Kenichi Okada
Tokyo Institute of Technology, Tokyo, Japan

2a. Reliability, Dynamic modeling, TCAD extraction with Neural Networks

Monday 3:40 PM - ***Valley of the Sun Ballroom AB***
Session Chair: Breandán Ó hAnnaidh, *Analog Devices*
Co-Chair: Saurabh Sirohi, *GlobalFoundries*

2a.1 (Invited)
3:40-4:20 PM – Characterization of Dynamic Large-Signal Operating Limits and Long-Term RF Reliability of SiGe HBTs
Christoph Weimer[1], Xiaodi Jin[1], Gerhard G. Fischer[2] and Michael Schröter[1]
[1] *Chair for Electron Devices and Integrated Circuits, Technische Universität Dresden, 01062 Dresden, Germany*
[2] *IHP, Leibniz-Institut für innovative Mikroelektronik, 15236 Frankfurt (Oder), Germany*

2a.2 (Student)
4:20-4:40 PM – Modeling Dynamic Lateral Current Crowding in SiGe HBTs
Sandip Ghosh[1], Shon Yadav[2], and Anjan Chakravorty[1]
[1] *Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai - 600036, India*
[2] *Global Foundries, Bengaluru, India*

2a.3 (Student)
4:40-5:00 PM – Recovery of Intrinsic Heterojunction Bipolar Transistors Profiles by Neural Networks
G. Caron[1, 2] A. Juditsky[2] N. Guitard[1] and D. C´eli[1]
[1] *STMicroelectronics, 38926 Crolles, France*
[2] *Laboratoire Jean Kuntzmann, 700 avenue Centrale, 38400 Saint Martin d’H`eres, France*

2b. mmW & THz Signal Generation

Monday 3:40 PM - ***Valley of the Sun Ballroom DE***
Session Chair: Vadim Issakov, *Technical University of Braunschweig*
Co-Chair: Frank Van Vliet, *TNO*

2b.1 (Student Paper)
3:40-4:00 PM – A SiGe D-Band x12 Frequency Multiplier with Gilbert Cell-Based Tripler
Justin Romstadt[1], Ahmad Zaben[1], Hakan Papurcu[1], Klaus Aufinger[2], Nils Pohl[1,3]
[1] *Ruhr-University Bochum, Universitatsstr. 150, D-44801 Bochum, Germany*
[2] *Infineon Technologies AG, Am Campeon 1-15, D-85579 Neubiberg, Germany*
[3]*Fraunhofer FHR, Fraunhoferstr. 20, D-53343 Wachtberg, Germany*

2b.2 (Student Paper)

4:00-4:20 PM A 280 GHz (x8) Frequency Multiplier Chain in 250 nm InP HBT Technology

Utku Soylu[1], Amirreza Alizadeh[1], Munkyo Seo[2], and Mark J. W. Rodwell[1]
[1] *Department of Electrical and Computer Engineering, University of California, Santa Barbara, USA*
[2] *Department of Electrical and Computer Engineering, Sungkyunkwan University, South Korea*

2b.3 (Student Paper)

4:20-4:40 PM – Broadband 0.4-4 THz Generation in 90nm SiGe BiCMOS

Sidharth Thomas, Sam Razavian, Wei Sun, Anthony D. Kim, Yu Wu, Benjamin S. Williams, Aydin Babakhani
Department of Electrical and Computer Engineering, University of California Los Angeles, CA USA

3a. Modeling of Scaling and Distributed Effects in III-V Devices

Tuesday 9:40 AM - ***Valley of the Sun Ballroom AB***
Session Chair: Subrata Halder, *Qorvo*
Co-Chair: Masaya Iwamoto, *Keysight Technologies*

3a.1 (Invited)

9:40-10:20 AM – A Review of Physics-Based Modeling of Millimeter-Wave Transistors Incorporating Wave-Propagation Effects

Soheil Nouri, Amirreza G. Avval, and Samir M. El-Ghazaly
Department of Electrical Engineering, University of Arkansas

3a.2 (Student)

10:20-10:40 AM – Characterization and Modeling of Thermal Coupling in Multi-Finger InP DHBTs

Markus Müller[1,2], Tobias Nardmann[1], Maximilian Froitzheim[1], and Michael Schröter[1,2]
[1] *Chair for Electron Devices and Integrated Circuits (CEDIC), TU Dresden, 01062 Germany*
[2] *SemiMod GmbH, 01159 Dresden, Germany*

3a.3

10:40-11:00 AM – Geometry scalable compact modeling of GaAs HBTs

Tobias Nardmann[3], Plamen Kolev[2], Nick Tao[4], and Michael Schröter[1]
[1] *Chair for Electron Devices and Integrated Circuits (CEDIC), TU Dresden, 01062 Germany*
[2] *Qualcomm Technologies, San Diego, 92121, USA*
[3] *formerly with CEDIC (now with Infineon Technologies, Dresden, Germany)*
[4] *formerly with Qualcomm Technologies, San Diego, 92121, USA*

3b. SiGe Technology

Tuesday 10:00 AM ***Valley of the Sun Ballroom DE***
Session Chair: Jack Pekarik, *GlobalFoundries*
Co-Chair: Jay John, *NXP Semiconductors*

3b.1

10:00-10:20 AM – Performance Improvements of SiGe HBTs in 90nm BiCMOS Process with f_T/f_{max} of 340/410 GHz

U. S. Raghunathan[1], S. Sirohi[1], V. Ruparelia[2], P. K. Sharma[2], D. P. Ioannou[3], V. Jain[4], H. K. Kakara[2], S. Gedela[2], V.Vanukuru[2],

P. Dongmo[1], C. Luce[1], R. Hazbun[1], R. Krishnasamy[1], J. Hwang[1], M. Levy[1], K. Welch[1], S. Liu[1], B. Cucci[1], S. Cole[1], J. Kantarovsky[1], A. Vallett[1], I. McCallum-Cook[1], M. Yu[1], R. Phelps[1], A. Divergilio[1], A. Sturm[1], M. Peters[1], S. Johnson[1], R. Rassel[1], M. Lagerquist[1], M. Kerbaugh[1], K. Newton[1], J. Pekarik[1], Q. Liu[1]
[1] GlobalFoundries, Essex Junction, VT 05452 USA
[2] GlobalFoundries, Bangalore, KA 560045 India
[3] GlobalFoundries, Hopewell Junction, NY 12533 USA
[4] GlobalFoundries, Malta, NY 12020

3b.2 (Invited)
10:20-11:00 AM – SiGe HBTs for Power Amplifiers in Front-End of Radio Communication Systems

Alvin Joseph[1], Vibhor Jain[2], John Pekarik[1], Ajay Raman[1], Shafi Syed[3], Liu Hang[4], Ned Cahoon[5], Randy Wolf[1], Venkat Vanukuru[6], Elan Veeramani[1], Beng Woon Lim[2], Uppili S. Raghunathan[1], Qizhi Liu[1], Yves Ngu[1]
[1] GlobalFoundries, Essex Junction, VT, USA
[2] GlobalFoundries, Malta, NY, USA
[3] GlobalFoundries, TX, USA
[4] GlobalFoundries, Singapore
[5] GlobalFoundries, MA, USA
[6] GlobalFoundries, Bangalore, India

4a. Electrothermal modeling and parameter extraction of SiGe HBTs

Tuesday 11:30 AM ***Valley of the Sun Ballroom AB***
Session Chair: Sadayuki Yoshitomi, *Mega Chips*
Co-Chair: Sebastien Fregonese, *Université de Bordeaux*

4a.1 (Student)
11:30-11:50 AM – Thermal impedance of SiGe HBTs: Characterization and modeling

Xiaodi Jin[1], Guangsheng Liang[1], Yves Zimmermann[1], Gerhard Fischer[2], Christoph Weimer[1],
Mario Krattenmacher[1], Yaxin Zhang[1], Michael Schröter[1]
[1] Chair for Electron Devices and Integrated Circuits, TU Dresden, 01069 Dresden, Germany
[2] IHP - Leibniz-Institut für innovative Mikroelektronik, 15236 Frankfurt (Oder), Germany

4a.2
11:50-12:10 PM – Impact of Layout Parasitics and Thermal Coupling on PA Performance and Ruggedness in SiGe HBTs

Saurabh Sirohi[1], Beng Woon Lim[2], Ajay Raman[1], and Frederick A. Anderson[1]
[1] GLOBALFOUNDRIES, 1000 River Street, Essex Junction VT 05452 USA
[2] GLOBALFOUNDRIES, 400, Stone Break Road Extn, Malta NY 12020 USA

4a.3 (Student)
12:10-12:30 PM – Extraction of Emitter Series Resistance Along With Collector and Thermal Resistances in Silicon Bipolar Transistors

Farzana Yasmin, Anjan Chakravorty, Nandita DasGupta, and Amitava DasGupta
Department of Electrical Engineering, Indian Institute of Technology Madras, India

4b. III-V Amplifiers

Tuesday 11:30 AM - ***Valley of the Sun Ballroom DE***
Session Chair: Michael Litchfield, *BAE Systems*
Co-Chair: Michael Roberg, *Qorvo*

4b.1
11:30-11:50 AM – A 1.8 GHz to 43 GHz Low Noise Amplifier with 4 dB noise figure in 0.1 um GaAs Technology

Mantas Sakalas and Paulius Sakalas
Baltic Institute of Advanced Technology, Vilnius, Lithuania

4b.2
11:50-12:10 PM – Reactively Matched 2-18 GHz Broadband GaN MMIC Driver Amplifier

Matthew Speir and Michael Litchfield
BAE Systems – ES Microelectronics, Merrimack, NH

4b.3
12:10 -12:30 PM – A Fully Integrated 3.2-4.7 GHz Doherty Power Amplifier in 300 mm GaN-on-Si Technology

Qiang Yu, Derek Thomson, Han Wui Then, Alvaro Latorre-Rey, Marko Radosavljevic, Michael Beumer, Pratik Koirala, Nicole Thomas, Nityan Nair, Heli Vora, Samuel Bader, and Said Rami
Intel Corporation, USA

5a. Advancements in GaN HEMT Modeling and Simulations

Tuesday 2:00 PM - ***Valley of the Sun Ballroom AB***
Session Chair: Lei Zhang, *NXP Semiconductors*
Co-Chair: Yueying Liu, *WolfSpeed*

5a.1 (Invited)
2:00-2:40 PM – Neural Network-based Methods for Microwave Active Device Modeling

Jinyuan Cui[1,2], Qi-Jun Zhang[2]
[1] Tianjin University, Tianjin, China
[2] Carleton University, Ottawa, Canada

5a.2 (Student)
2:40-3:00 PM – MVSG GaN-HEMT Model: Approach to Simulate Fringing Field Capacitances, Gate Current De-biasing, and Charge Trapping Effects

Ryan Fang[1], Dylan Ma[1], Ujwal Radhakrishna[2], and Lan Wei[1]
[1] Department of Electrical and Computer Engineering, University of Waterloo
[2] Kilby Research Labs, Texas Instrument Inc.

5a.3 (Student)
3:00 -3:20 PM – Significance of Equivalent Channel Temperature in Compact Modeling of GaN HEMTs

Sruthi M P, Nidhin K, Ajay Shanbhag, Deleep R Nair, Anjan Chakravorty, Nandita DasGupta, and Amitava DasGupta
Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai 600036 India

5a.4
3:20 -3:40 PM – Numerical Optimization of ON-Resistance and Transconductance in Depletion-mode and Enhancement-mode GaN HEMTs

Ivan Berdalovic, Mirko Poljak, and Tomislav Suligoj
Faculty of Electrical Engineering and Computing, University of Zagreb, 10000 Zagreb, Croatia

5b. High-Performance Circuits for Communications and Quantum Applications

Tuesday 2:00 PM - ***Valley of the Sun Ballroom DE***
Session Chair: Munehiko Nagatani, *NTT*
Co-Chair: Craig Steinbeiser, *Qorvo*

5b.1 (Student)
2:00-2:20 PM – Improved Signal Integrity at 64 Gbps in a 130-nm SiGe Optical Receiver With Through-Silicon Vias
Ghazal Movaghar, Junqian Liu, James Dalton, Luis A. Valenzuela, Clint L. Schow, James F. Buckwalter
Dept. o Elec. and Comp. Engineering, University of California, Santa Barbara, CA, USA

5b.2 (Student)
2:20 -2:40 PM – Lumped Ultra-Broadband Linear Driver in 130 nm SiGe SG13G3 Technology
Festim Iseini[1], Andrea Malignaggi[1], Falk Korndorfer[1], Mesut Inac[1], and Gerhard Kahmen[1,2]
[1] IHP-Leinbiz-Institut fur innovative Mikroelectronik, Frankfurt, Germany
[2] Institute of Electrical Engineering and Information Science, Brandenburg Technical University Cottbus, Cottbus, Germany

5b.3 (Student, Late News)
2:40 -3:00 PM – A 0.03 mm2 Inductorless 50 Gb/s Multiplexer for Josephson Arbitrary Waveform Synthesizers
Yerzhan Kudabay, and Vadim Issakov
Institute for CMOS Design, TU Braunschweig, Braunschweig, Germany

5b.4 (Late News)
3:00 -3:20 PM – High Linearity Ka-band InP HBT MMIC Amplifier with 19.8:1 IP3/Pdc LFOM at 48 GHz
Kevin W. Kobayashi, Paul Partyka, Tim Howle, Tony Sellas, Leonard Hayden
Qorvo Inc, USA

6a. Bipolar Device Physics

Tuesday 4:10 PM - ***Valley of the Sun Ballroom AB***
Session Chair: Martin Claus, *Infineon*
Co-Chair: Guanghai Ding, *Analog Devices*

6a.1 (Student)
4:10-4:30 PM – Performance vs. Reliability Tradeoffs of Medium Breakdown and High Performance Cascode Amplifier Cells
Harrison P. Lee, Arya Moradinia, Jeffrey W. Teng, Nelson E. Sepulveda-Ramos, and John D. Cressler
School of Electrical and Computer Engineering, Georgia Tech, Atlanta, GA 30332 USA

6a.2 (Student)
4:30-4:50 PM – Improved Electrical Reliability and Performance Enhancements in SiGe HBTs Using Dummy BEOL Metal Layers
Nelson E. Sepulveda-Ramos, Jeffrey W. Teng, Harrison P. Lee, and John D. Cressler
School of Electrical and Computer Engineering, Georgia Tech, Atlanta, GA 30332 USA

6a.3 (Invited)
4:50-5:30 PM – Physics, Characterization and Modeling of RF Linearity in SiGe HBT and FinFET Technologies

Guofu Niu
Alabama Micro and Nanoelectronics Science and Technology Center, Auburn University, Auburn, AL 36849, USA

6b. III-V mmW Power Amplifier Technologies

Tuesday 4:10 PM - ***Valley of the Sun Ballroom DE***
Session Chair: Harris P Moyer, *HRL Laboratories, LLC.*
Co-Chair: Nils Pohl, *Ruhr-University Bochum*

6b.1 (Invited)
4:10-4:50 PM – Sub-100nm GaN/Si MMIC processes for 6G telecommunications

Rémy LeBlanc, Peter Frijlink, Marc Rocchi
OMMIC SAS, Limeil Brévannes, France

6b.2
4:50-5:10 PM – A 29-dBm, 34% PAE E-Band Dual-Input Doherty Power Amplifier Using 40-nm GaN Technology

Toshifumi Nakatani[1], Mohammad Ali Zolfaghari[1], Jonmei J. Yan[1], Peter M. Asbeck[2]
[1] *MaXentric Technologies LLC*
[2] *Electrical and Computer Engineering, University of California, San Diego, USA*

6b.3
5:10 -5:30 PM – A 220-294 GHz Power Amplifier with 10-dBm Psat and 2.2% PAE in 250-nm InP DHBT

Teruo Jyo[1], Hiroshi Hamada[1], Munehiko Nagatani[1], Hitoshi Wakita[1], Ibrahim Abdo[1], Miwa Mutoh[1],Yuta Shiratori[1], Kenichi Okada[2], Atsushi Shirane[2], Hiroyuki Takahashi[1]
[1] *NTT Device Technology Labs, NTT Corporation, Kanagawa, Japan*
[2] *Tokyo Institute of Technology, Tokyo, Japan*

7a. High Frequency GaN and UWBG Devices

Wednesday 8:30 AM - ***Valley of the Sun Ballroom AB***
Session Chair: Kanin Chu, *BAE Systems*
Co-Chair: Hiroshi Yamamoto, *Sumitomo Electric Industries, Ltd.*

7a.1 (Invited)
8:30-9:10 AM – Performance Improvement and Layout Design Comparison of AlGaN/GaN HEMT for Ka- Q- and V-band Applications

Keiichi Matsushita, Chih-Yuan Chan, Ju-Hsien Lin, Sheng-Wen Peng, Hung-Kuan Lo, Yu-Syuan Lin, Cheng-Kuo Lin
WIN Semiconductors Corp, Taoyuan City 333, Taiwan

7a.2
9:10-9:30 AM – Capacitance Engineering of GaN HEMT Technologies with Recessed Field Plate

Kyle M. Bothe, Matthew R. King, Jia Guo, Yueying Liu, Saptha Sriram, Jeremy Fisher, Scott T. Sheppard, and Basim Noori
Wolfspeed, Durham, USA

7a.3 (Invited)
9:30-10:10 AM – Ultrawide Bandgap Nitride Semiconductor Heterojunction Field Effect Transistors
Wu Lu
Dept. of Electrical and Computer Engineering, The Ohio State University, Columbus, OH USA

7b. Advancements in SiGe Circuit Designs
Wednesday 8:50 AM - ***Valley of the Sun Ballroom DE***
Session Chair: Jim Carroll, *Akash Systems*
Co-Chair: Arun Paidimarri, *IBM*

7b.1 (Student)
8:50-9:10 AM – A 5-GHz Injection-Locked Delay Cell with 10-25 ns Adjustable Group-Delay in a 130-nm SiGe BiCMOS Technology
A. S. Nazhad[1], A. Alizadeh[1], M. Frounchi[2], J. D. Cressler[2], B. Bakkaloglu[1], S. Kiaei[1]
[1]*Arizona State University, Arizona, USA*
[2]*Georgia Institute of Technology, Georgia, USA*

7b.2 (Student)
9:10-9:30 AM – 13 GHz PA with Amplitude-Modulation for Entanglement Generation in Multi-Qubit 171Yb+ Gates of an Ion-Trapped Quantum Computer
Peter Toth, Lasse Cordes, and Vadim Issakov
Institute for CMOS Design, TU Braunschweig, Germany

7b.3
9:30-9:50 AM – A Static Frequency Divider up to 163 GHz in SiGe-BiCMOS Technology
Florian Vogelsang[1], Christian Bredendiek[2], Jan Schopfel[1], Holger Rucker[3], and Nils Pohl[1,2]
[1] *Institute of Integrated Systems, Ruhr University Bochum, Germany*
[2] *Fraunhofer Institute for High Frequency Physics and Radar Techniques, Germany*
[3] *IHP - Leibniz-Institut fur innovative Mikroelektronik, 15236 Frankfurt (Oder), Germany*

7b.4
9:50 - 10:10 AM – A Multiple Input and Gain Adjustable Phase Detector in 130 nm SiGe BiCMOS Technology
Rabia Fatima Riaz[1], Manu Viswambharan Thayyil[1], Jens Wagner[12], Lucas Wetzel[3], Dimitrios Prousalis[3], and Frank Ellinger[12]
[1] *Chair for Circuit Design and Network Theory, Technishe Universitat Dresden, Germany*
[2] *Centre for Tactile Internet with Human-in-the-Loop, Technishe Universitat Dresden, Germany*
[3] *Max Planck Institute for the Physics of Complex Systems, Dresden, Germany*

8a. Late News 1

Wednesday 10:40 AM - ***Valley of the Sun Ballroom AB***
Session Chair: Rob Howell, *Northrop Grumman*
Co-Chair: Breandán Ó hAnnaidh, *Analog Devices*

8a.1 (Student)
10:40-11:00 AM – A 180-220-GHz, 12.7-dBm peak Psat and 17.3% peak PAE Power Amplifier in 250-nm InP HBT

Jeff Shih-Chieh Chien, Wonho Lee and James F . Buckwalter
Dept.Electrical and Computer Engineering, University of California, Santa Barbara, USA

8a.2 (Student)
11:00-11:20 AM – The Load-Modulated Linearizer: A Technique for Intermodulation Cancellation in PA Systems

Anton N. Atanasov[1], Wasam R. A. Mukhtar Ahmad[1], Mark S. Oude Alink[1], Frank E. van Vliet[1,2]
[1] Integrated Circuit Design, University of Twente, Enschede, Netherlands
[2] Defence, Safety & Security, TNO, The Hague, Netherlands

8a.3
11:20-11:40 AM – Low Loss, High Linearity Switches for Wideband Applications

Matt Torpey and Austin Tucker
Northorp Grumman Corporation (Mission Systems), Linthicum Maryland 21090, USA

8b. Late News 2

Wednesday 10:40 AM - ***Valley of the Sun Ballroom DE***
Session Chair: Nils Pohl, *Ruhr-University Bochum*
Co-Chair: Tomislav Suligoj, *University of Zagreb*

8b.1 (Student)
10:40-11:00 AM – A 42.5–51.0 GHz SiGe BiCMOS Integrated Tunable Bandpass Filter and Attenuator

Arya Moradinia[1], Clifford D. Cheon[2], Christopher T. Coen[3], Nelson E. Lourenco[3], Adilson S. Cardoso[3,4], and John D. Cressler[1]
[1] School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA
[2] Broadcom Inc., San Jose, CA USA
[3] Georgia Tech Research Institute, Atlanta, GA USA
[4] Raytheon Technologies, El Segundo, CA USA

8b.2 (Student)
11:00-11:20 AM – A 0.4 THz Efficient OOK/FSK Wireless Transmitter Enabling 3 Gbps at 20 meters

Sam Razavian, Sidharth Thomas, Mostafa Hosseini, Aydin Babakhani
University of California, Los Angeles, CA, USA

8b.3
11:20-11:40 AM – Design of 20-28 GHz GaAs Phase Shifter MMIC and Small Signal Validation using MVS-GaAs Model

Pilsoon Choi[1], Ryan Fang[2], Lan Wei[2], Slim Boumaiza[2], Ujwal Radhakrishna[3], and Eugene Fitzgerald[1]
[1] Massachusetts Institute of Technology, Cambridge, MA 02139, USA
[2] University of Waterloo, Waterloo, ON N2L 3G1, Canada
[3] Texas Instrument, Santa Clara, CA 95051, USA

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RF and Microwave ICs

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Michael Roberg	Qorvo
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Jim Carroll	Akash Systems
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The 2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) is the IEEE-approved merger of the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) and the Compound Semiconductor IC Symposium (CSICS). BCICTS is the forum for developments in bipolar, BiCMOS, and com-pound semiconductor circuits, devices, and technology. Coverage includes all aspects of the technology, from materials, device fabrication, device phenomena, TCAD modeling, compact modeling, integrated circuit design, testing, and system applications. A wide range of integrated circuit technologies are covered including CMOS, bipolar and field-effect transistors realized in materials such as SiGe, GaAs, GaN, InP, SiC. The latest results in wireless, analog, RF, microwave, high-speed digital, mixed signal, optoelectronic, millimeter wave, and THz integrated circuits are embraced. Subject area groupings are:

HIGH-SPEED DIGITAL, MIXED-SIGNAL, AND OPTOELECTRONIC ICs Mixed analog/digital ICs - Digital ICs - (high-speed) DACs and ADCs - Networking ICs, MUX/DEMUX, Clock and data recovery, Decision circuits, Equalizers - Optical data links, Laser and modulator drivers, optoelectronics and photonics ICs

ANALOG, RF, AND MICROWAVE ICs
Op amps - Voltage references and regulators - Integrated filters - Sensors and actuators - RF circuits and systems - Radio and transceiver subsystems - LNAs - AGCs - Mixers - Voltage controlled oscillators - Frequency synthesizers - Power amplifiers - RF switches - Noise and distortion suppression - RF Packaging - Integrated RF passives. Analog, RF, power conversion, High-voltage ICs - Biomedical electronics - Power Management ICs - Energy harvesting ICs - Motor controls - Analog subsystems within a VLSI chip - Packaging of high-performance ICs.

mm-WAVE AND THZ ICs
Millimeter - wave circuits and systems - THz circuits and systems. MM-Wave switches and amplifiers. Phased-array antenna circuits

DEVICE PHYSICS:
New device physics phenomena in Si, SiGe, SiC, GaN, MOS, and III-V HBTs and FETs - Device design issues and scaling limits - Hot electron effects and reliability physics - Transport and high field phenomena - Noise - Linearity/Distortion - Novel measurement techniques - Operation in extreme environments (low/high temperatures, radiation effects), and ESD phenomena.

MODELING AND SIMULATION
Improved silicon-based BJT and HBT models and physics-based modelling techniques - Improved III-V HBT and FET models and physics-based modelling techniques - Parameter extraction methods and test structures - High-frequency measurement, calibration and de-embedding techniques - RF and thermal simulation techniques - Modelling of passives, interconnect and packages - Statistical modelling - Device, process and circuit simulation - CAD/modelling of power devices - Packaging of power devices.

PROCESS AND DEVICE TECHNOLOGY

Device and IC manufacturing processes, testing methodologies, & reliability - Integration of III-V devices on Si - High performance devices such as GaN power conversion devices - near-THz SiGe HBTs & InP HEMTs - Novel devices such as tunnel FETs (TFETs) - carbon nanotubes, MEMS, graphene & diamond transistors. Optoelectronic and photonic devices such as optical modulators, lasers, photodetectors, and Silicon Photonics - Thermal management technologies, thermal simulation - Advanced packaging of high-power devices and ICs. Advances in processes and device structures demonstrating high speed, low power, low noise, high current, high voltage, etc. BiCMOS processes - Advanced process techniques - Si and SiC homojunction bipolar/BiCMOS devices and SiGe heterojunction bipolar/BiCMOS devices - Manufacturing solutions related to Bipolar and BiCMOS yield improvements - Fabrication of high-performance passive components, sensors, and MEMs - Process technology related to discrete and integrated bipolar/BiCMOS power devices - IGBT, RF power devices. Wide bandgap bipolar devices (e.g., SiC) and related process technology - 3D Integration - Reliability and testing for IC manufacturing

IMPORTANT DATES

Friday May 5, 2023 – Abstracts Due
Monday, July 3, 2023 – Decision E-mail Sent
Thursday, August 31, 2023 – Final Manuscript Due

Authors must submit an abstract (not more than 4 pages including figures and other supporting material) of results not previously published or not already accepted by another conference. Papers will be selected on the basis of the abstract.

The abstract must concisely and clearly state:

a) The purpose of the work
b) What specific new results have been obtained
c) How it advances the state-of-the-art or the industry
d) References to prior state-of-the-art
e) Sub-committee preference:
    - Analog, RF, and Microwave ICs
    - Device Physics
    - High-Speed Digital, Mixed-Signal, & Optoelectronic ICs
    - Modeling & Simulation
    - mm-Wave and THz ICs
    - Process & Device Technology

Abstracts must include: title, author(s) name(s) and affiliation(s), corresponding authors' postal and e-mail addresses, and telephone numbers. The committee will honor the authors' committee preference but reserves the right to review the paper in other categories.

Company and governmental clearances must be obtained prior to submission of the abstract.

Accepted work may be used for publicity purposes. Portions of the abstracts may be quoted in articles publicizing the Symposium. Please note on the abstract if this is not acceptable.

Abstracts (PDF only) must be submitted electronically.

Authors will be informed of a decision by July 3, 2023. Authors of accepted papers are required to submit a 4-page camera-ready PDF by August 31, 2023 for inclusion in the Symposium Digest.

Further questions on abstract submission may be addressed to the Symposium Technical Chair:

Dr. Breandan O hannaidh
BE, PhD, MIEEE
Device Modeling & Characterisation Lab Manager,
ADLK Device Technology, Analog Devices
Email: breandan.ohannaidh@analog.com

Symposium information, including abstract submission instructions and a link to the abstract submission system is available on the BCICTS website at: http://www.bcicts.org

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