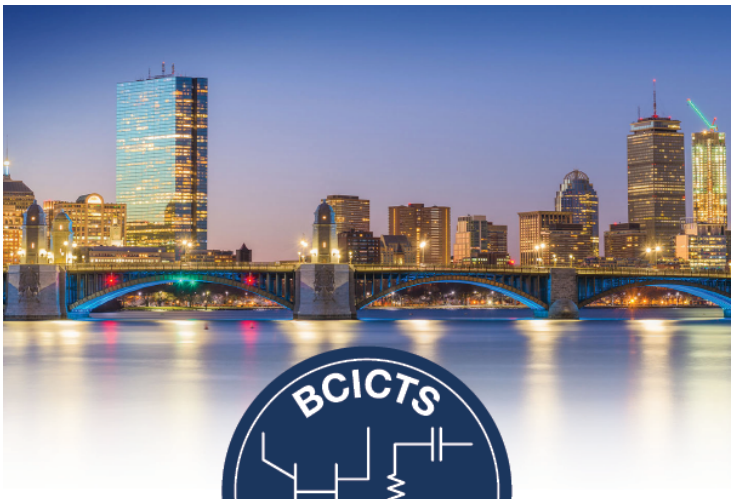


2026 BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)

October 11-14, 2026
Boston Massachusetts, USA

CONFERENCE PROGRAM

Sponsored by
The Electron Devices Society of The Institute of Electrical and Electronic Engineers

In Cooperation with
The IEEE Solid - State Circuits Society and The IEEE Microwave Theory & Technology Society

www.bcicts.org

WELCOME FROM THE BCICTS 2026 CO-CHAIRS

With great pleasure, we invite you to participate in the 2026 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS). The ninth edition of this premier in-person symposium will be held Sunday, October 11 through Wednesday, October 14, 2026, at The Westin Copley Place in Boston, Massachusetts, USA. BCICTS provides an outstanding opportunity for the engineering and technical community to reconnect professionally and personally, meet new colleagues, renew longstanding relationships, and stay informed on the latest developments and trends across microelectronics.

This year, BCICTS continues its long tradition of bringing together distinguished experts to present their latest results in bipolar, Si/SiGe BiCMOS, and compound semiconductor circuits, devices, and technologies. There are few venues worldwide where attendees can experience leading-edge advances in bipolar and BiCMOS devices and technology, 5G/6G ICs, GaN HPAs, InP THz PAs, optical CMOS/SiGe transceivers, GaN HEMT power devices, modeling and simulation, and device physics, all within a single technical program.

BCICTS features presentations from contributors worldwide covering all aspects of semiconductor technologies. Topics span process technology, device innovations, TCAD and compact modeling, IC design and testing, high-volume manufacturing, and system-level applications. The symposium will also showcase the latest results in RF, microwave, millimeter-wave, THz, analog and mixed-signal, and optoelectronic integrated circuits.

A highlight of this year's symposium is the opportunity to participate in one of two exceptional educational offerings on October 11:

- The BCICTS Short Course, taught by leading industry and academic experts, is designed for experienced professionals seeking a comprehensive understanding of the latest technology trends, challenges, and innovations shaping the industry.
- The BCICTS Primer provides an accessible introduction to key concepts and technologies, making it an ideal starting point for engineers, students, and professionals entering the field or expanding into new technical areas.

Whether you are looking to deepen your expertise through the advanced Short Course or build a strong foundation through the Primer, these programs offer valuable learning opportunities and are excellent additions to your symposium experience. We encourage attendees to register early and take advantage of these unique educational sessions. Additional details are available on the BCICTS website.

In addition, BCICTS 2026 will host two industry panels on Monday, followed by our popular Exhibition Reception, providing further opportunities for technical discussion, networking, and collaboration.

We would like to thank the many dedicated volunteers on the BCICTS Technical Program Committee, as well as the generous support of the IEEE Electron Devices Society, IEEE Microwave Theory and Technology Society, and IEEE Solid-State Circuits Society.

We look forward to welcoming you to Boston and engaging with participants from around the world as we continue the tradition of technical excellence that defines BCICTS.

Jack Pekarik
GlobalFoundries
Symposium Chair

Michael Roberg
Qorvo, Inc.
Symposium Co-Chair

KEY EVENT INFORMATION

Meeting Locations:
*Registration is required for attendance

- **Registration:** Essex Ballroom Foyer
- **Sunday:** Short course, Essex Center
- **Sunday:** Primer, Essex Center
- **Monday - Wednesday:**
  - **General Session:** Essex South
  - **Session A:** Essex North & Center
  - **Session B:** Essex South
  - **Exhibition:** St. George ABC & Essex Foyer
  - **Attendee Lounge & Speaker Ready Room:** St. George D

Conference Networking & Social Events:
Several networking events have been arranged to promote informal social interactions among conference participants. Event details are listed below for your reference:

Monday, October 12:

Exhibitor Reception: 5:45 PM - 7:45 PM
Location: St. George ABC & Essex Ballroom Foyer

Tuesday, October 13:

Exhibitor Breakfast: 7:30 AM - 8:30 AM
Exhibitor Luncheon: 12:00 PM - 1:30 PM
Location: St. George ABC & Essex Ballroom Foyer

Wednesday, October 14:

Closing Reception: 3:30 PM – 4:00 PM
Location: Essex Ballroom Foyer

Registration Desk Hours:
Sunday - Tuesday: 7:30 AM - 5:00 PM
Wednesday: 7:30 AM - 3:30 PM

We're looking forward to seeing you in Boston, Massachusetts!

If you have any questions, please feel free to contact Catherine Shaw:

Catherine Shaw, CMP
Executive Director, Meetings and Events (BCICTS)
Phone: 732-501-3334
E-mail: cs@cshawevents.com

2026 BCICTS SCHEDULE AT A GLANCE

SUNDAY – OCTOBER 11	
SHORT COURSE A.I.-Driven Circuit Design: Theory, Tools, and Practice **Essex Center**	
7:30 AM **8:30 AM**	Registration for Short Course Only **Essex Ballroom Foyer**
7:30 AM **8:15 AM**	Breakfast for Short Course Only **Essex Ballroom Foyer**
8:15 AM **8:30 AM**	Welcome & Speaker Introduction, Saurabh Sirohi, GlobalFoundries **Essex Center**
8:30 AM **9:30 AM**	Short Course Session 1 – Prof. Sensen Li, Univ. of Texas at Austin AI-Assisted PA Design: Methods and Practice **Essex Center**
9:30 AM **9:45 AM**	Coffee Break for Short Course Only **Essex Ballroom Foyer**
9:45 AM **10:45 AM**	Short Course Session 2 – Dr. Jason Blocklove, New York University, Tandon Auto-Chip: Towards Fully Autonomous Chip Design Flows with AI Agents **Essex Center**
10:45 AM **11:00 AM**	Coffee Break for Short Course Only **Essex Ballroom Foyer**
11:00 AM **12:00 PM**	Short Course Session 3 — Dr. Mehdi Saligane, Brown University Rethinking Chip Design in the Age of A.I. **Essex Center**
12:00 PM **12:15 PM**	Adjourn and Feedback **Essex Center**
12:15 PM **1:00 PM**	Lunch **Essex North**
PRIMER Millimeter-wave Design, Packaging and Measurements **Essex Center**	
8:45 AM **1:30 PM**	Registration for Primer Course Only **Essex Ballroom Foyer**
1:00 PM **1:10 PM**	Welcome & Speaker Introduction, Leo Vera **Essex Center**
1:10 PM **2:10 PM**	Primer Lecture 1 — Dr. Akshay Visweswaran, Nokia Bell Labs Millimeter-Wave FMCW Radar **Essex Center**
2:10 PM **2:25 PM**	Coffee Break for Primer Only **Essex Ballroom Foyer**
2:25 PM **3:25 PM**	Primer Lecture 2 — Prof. Madhavan Swaminathan, Penn State University Advanced Packaging for mm-Wave Systems **Essex Center**
3:25 PM **3:40 PM**	Coffee Break for Primer Only **Essex Ballroom Foyer**
3:40 PM **4:40 PM**	Primer Lecture 3 — Dr. Luciano Boglione, Boeing Measuring Noise Parameter: An Alternative, Size-Based Approach for On-Wafer Device Characterization **Essex Center**
4:40 PM **5:00 PM**	Primer Wrap-Up **Essex Center**

2026 BCICTS SCHEDULE AT A GLANCE

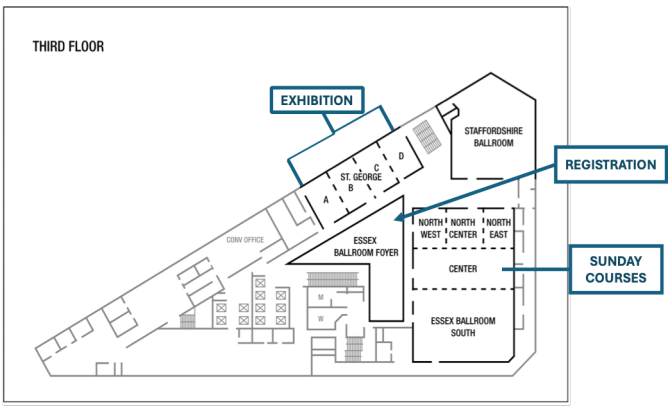
MONDAY – OCTOBER 12		
7:30 AM **5:00 PM**	Registration **Essex Ballroom Foyer**	
8:30 AM **9:30 AM**	Continental Breakfast **Essex Ballroom Foyer**	
9:30 AM **10:00 AM**	Welcome and Announcements **Essex Ballroom South**	
10:00 AM **12:00 PM**	Plenary Session **Essex Ballroom South**	
12:00 PM **1:30 PM**	Lunch **Self-Arrangement**	
1:30 PM **3:10 PM**	1a. Compound Advanced Devices and Technology **Essex North & Center**	1b. Next-gen BiCMOS and AI for Inverse Design **Essex South**
3:10 PM **3:40 PM**	Coffee Break Sponsored by **Qorvo** **Essex Ballroom Foyer**	
3:40 PM **4:40 PM**	Panel 1 — WIE/YP Panel: AI in Engineering Design: Opportunities, Challenges, and the Road Ahead **Essex South**	
4:45 PM **5:45 PM**	Panel 2 — The GaN-on-Si Revolution: Hype or Reality? **Essex South**	
5:45 PM **7:45 PM**	Exhibition Reception **St. George ABC & Essex Foyer**	

TUESDAY – OCTOBER 13		
7:30 AM **5:00 PM**	Registration **Essex Ballroom Foyer**	
7:30 AM **8:30 AM**	Breakfast & Exhibition **St. George ABC & Essex Foyer**	
8:30 AM **2:30 PM**	Exhibition **St. George ABC & Essex Foyer**	
8:30 AM **10:10 AM**	2a. Designing with GaN: LNAs, PAs, and Beyond **Essex North & Center**	2b. High-Performance Circuits for Optical Communications **Essex South**
10:10 AM **10:40 AM**	Sponsored Coffee Break **St. George ABC & Essex Foyer**	
10:40 AM **12:00 PM**	3a. Modeling of Polarization and Memory Effects in GaN **Essex North & Center**	3b. Transmitter Circuits for Optical Communications **Essex South**
12:00 PM **1:30 PM**	Exhibition Lunch **St. George ABC & Essex Foyer**	
1:30 PM **3:30 PM**	4a. mmW Receiver and Transmitter Technologies **Essex North & Center**	4b. Advances in Compact & Analytical Modeling; RF & mm-wave Measurement Tools and Techniques **Essex South**
3:30 PM **4:00 PM**	Sponsored Coffee Break **Essex Ballroom Foyer**	
4:00 PM **6:00 PM**	5a. Ultra High Frequency Circuit and System Design Techniques **Essex North & Center**	5b. Analog ICs **Essex South**

2026 BCICTS SCHEDULE AT A GLANCE

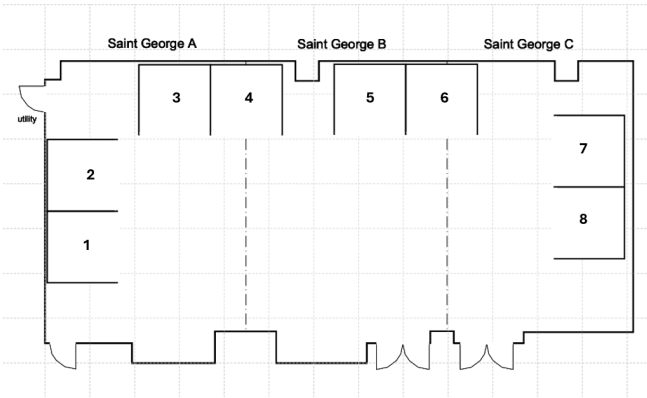
WEDNESDAY – OCTOBER 14		
7:30 AM **3:30 PM**	Registration **Essex Ballroom Foyer**	
7:30 AM **8:30 AM**	Breakfast **Essex Ballroom Foyer**	
8:30 AM **10:10 AM**	6a. SiGe, GaAs, InP, GaN, and Cryogenic Circuits: An Evolutionary Perspective **Essex North & Center**	6b. Next Generation High-Frequency Device Modeling **Essex South**
10:10 AM **10:40 AM**	Coffee Break Sponsored by **Texas Instruments** **Essex Ballroom Foyer**	
10:40 AM **12:20 PM**	7a. mm-Wave III-V IC Measurements and Power Generation **Essex North & Center**	7b. High Performance SiGe BiCMOS and Electrostatic Doped Devices **Essex South**
12:20 PM **1:50 PM**	Lunch **Self-Arrangement**	
1:50 PM **3:30 PM**	8a. Late News **Essex North & Center**	8b. Late News **Essex South**
3:30 PM **4:00 PM**	Closing Reception Sponsored by **Global Foundries** **Essex Ballroom Foyer**	

HOTEL MAP



EXHIBITION FLOORPLAN

St. George ABC



BOOTH #	COMPANY NAME
1	StratEdge Corporation
2	MPI Corporation
3	Virginia Diodes
4	Presidio Components
5	Maury Microwave
6	FormFactor

ADDITIONAL INFORMATION

REGISTRATION Complete registration information is contained in the centerfold of this booklet as well as on the conference's web page (https://bcicts.org) Please use the website to register. The advanced registration deadline is **September 8**. All conference activities are included in the registration fees (technical sessions, coffee breaks, Monday exhibition reception, Tuesday exhibition breakfast)

CONFERENCE SOCIAL EVENTS Several events have been arranged to promote informal social interactions among conference participants.

TUTORIAL / SURVEY TALKS Tutorial talks given by invited experts are intended to give a broad overview of a given subject with a critical review of technology and applications. They are twice the length of the usual contributed talk with longer abstracts in the Proceedings.

MEMBERS OF THE PRESS: You are welcome to attend BCICTS. Admission is free. Please email Catherine Shaw, CMP, Executive Conference Director at: cs@cshawevents.com for pre-registration and approval by our Executive Committee.

RECRUITING: Intensive recruitment undermines the purposes for which the BCICTS was established and is contrary to IEEE policy.

BEST STUDENT PAPER AND BEST PAPER AWARDS
The BCICTS Best Paper Award recognizes and promotes high quality contributions to scholarly research among professionals who author and present papers at the conference. All papers submitted in non-student category are eligible for consideration for the Best Paper Award.

The BCICTS Best Student Paper Award recognizes and promotes outstanding research led by students. The Best Student Paper Award the following criteria: 1) the student must have carried out a substantial part of the research reported in the paper, 2) the student must be the first author and must present the paper at the conference, 3) the paper must be identified as a student paper during submission of the paper.

Eligible papers have been evaluated by the Best Paper Award Committee, and the notifications will be sent out after the conference.

OUR SPONSORS
BCICTS is sponsored by the IEEE Electron Devices Society (EDS) in co-operation with the IEEE Solid – State Circuits Society (SSCS) and the IEEE Microwave Theory & Technology Society (MTT).

MEETINGS & SESSIONS SCHEDULE DETAILS

SUNDAY

BCICTS 2026 SHORT COURSE
ESSEX CENTER

Time: 8:15 AM – 12:15 PM
Topic: AI-Driven Circuit Design: Theory, Tools and Practice

Speakers:

- Dr. Sensen Li, University of Texas at Austin
- Jason Blocklove, NYU Tandon School of Engineering
- Dr. Mehdi Saligane, Brown University

7:30 – 8:15 AM **Breakfast (Short Course Only)**

8:15 – 8:30 AM **Welcome**
Saurabh Sirohi, GlobalFoundries

8:30 – 9:30 AM **AI-Assisted PA Design: Methods and Practice**
Instructor: Dr. Sensen Li, University of Texas at Austin

Abstract: Artificial intelligence is creating new opportunities to improve the productivity, design-space exploration, and performance of radio-frequency power amplifiers. This short course presents methods and practical considerations for integrating machine learning into the PA design workflow, progressing from passive-network modeling and inverse synthesis to model-driven active–passive co-design. The course first examines the limitations of conventional PA development, where active devices and passive networks are often optimized through repeated circuit simulation, layout refinement, electromagnetic simulation, and manual tuning. It then introduces physics-augmented surrogate modeling for multilayer, multiport passive structures, including layout representations, U-Net-based S-parameter prediction, causality and passivity constraints, and Bayesian-optimization-based synthesis of low-loss input, interstage, and output matching networks.

Building on these techniques, the course presents a model-driven framework that employs surrogate models for both active circuits and passive structures and formulates PA design as a structured bi-level co-optimization problem. A passive-initiated strategy confines the optimization to physically realizable boundary conditions, such as loading impedances, for the active devices, while circuit-level analytical relationships combine active and passive performance without requiring repeated full co-simulation. The framework jointly determines transistor dimensions, bias conditions, stability circuitry, loading impedances, and passive geometries while optimizing gain, output power, efficiency, bandwidth, impedance matching, and stability. Its successful application to a synthesized 28-GHz PA, together with its extensibility to other RFIC blocks, demonstrates the scalability and accuracy of the proposed approach. Finally, measured results from a D-band InP PA prototype with fully AI-generated passive networks illustrate the transition from AI-assisted synthesis to fabricated hardware. Practical discussions will address dataset generation, model validation, optimization formulation, EM and circuit verification, design-rule constraints,

and the role of designer knowledge in developing reliable and interpretable AI-assisted PA design flows.

Sensen Li received the B.Eng. (Hons.) from Zhejiang University and the Ph.D. from the Georgia Institute of Technology. He is currently an Assistant Professor in the Department of Electrical and Computer Engineering at The University of Texas at Austin, where he directs the UT-Austin Circuits and Electromagnetics (UT-ACE) Lab. Previously, he was with Samsung Research, working on 6G wireless systems. His research focuses on analog, RF, and mm-wave integrated circuits and systems for wireless communication and sensing, as well as AI-enabled RFIC design automation.

Dr. Li's research group received the 2025 ISSCC Jack Kilby Award for Outstanding Student Paper and the 2025 IEEE Microwave Prize, along with multiple other recognitions, including IEEE IMS Best Paper Finalist and First and Second Place in the Texas Wireless Symposium Student Research Competition. He is also a recipient of the 2018 IEEE RFIC Best Paper Award, with additional best paper recognitions at IEEE RFIC, IMS, and CICC. Dr. Li serves on the Technical Program Committees of IEEE IMS, CICC, and RFIC, and is an Associate Editor for the IEEE Transactions on Microwave Theory and Techniques (T-MTT).

9:30 – 9:45 AM Coffee Break

9:45 – 10:45 AM Auto-chip: Towards fully autonomous chip design flows with AI agents
Instructor: Jason Blocklove, NYU Tandon School of Engineering

Abstract: With the continued and rapid growth of generative AI technologies in recent years, it has become imperative that we determine how best it can be used to aid the efforts of hardware engineers. This short course will detail the history of using large language models for digital hardware design, and provide demonstrations and hands-on activities for how best LLMs can be used in this field. We will cover simple conversational methods of LLM use, as well as fully automated methods which enable the most recent and capable models to generate hardware from just a system specification and testbench. We will also detail the current digital hardware security concerns that LLMs pose, and the current methods we have to mitigate these potential issues.

Jason Blocklove is a Ph.D. candidate in Electrical and Computer Engineering at the NYU Tandon School of Engineering, advised by Dr. Ramesh Karri. He previously completed his B.S/M.S. in Computer Engineering at the Rochester Institute of Technology, and following that was employed for a time at the Johns Hopkins University Applied Physics Lab before returning to academia. His research focuses primarily on leveraging generative AI for hardware design and security, as well as how generative AI can be used for hardware design education. He has also previously focused on additive manufacturing and PCB security.

10:45 – 11:00 AM Coffee Break

11:00 – 12:00 PM Rethinking Chip Design in the Age of A.I.
Instructor: Dr. Mehdi Saligane, Brown University

Abstract: AI is beginning to transform circuit design by assisting engineers across specification, topology generation, sizing, layout, verification, and design-space exploration. This lecture will provide a practical overview of emerging AI-assisted methodologies for analog, mixed-signal, and custom circuit design. It will discuss how large language models, reinforcement learning, and optimization techniques can interact with conventional EDA tools and physics-based

simulation to generate and refine circuits while maintaining design-rule and performance constraints. Examples will illustrate natural-language-to-layout workflows, AI-guided circuit optimization, automated layout generation, and rapid PPA estimation. The lecture will also examine current limitations, including data scarcity, verification, generalization across technologies, and designer trust and outline opportunities for combining domain knowledge, open-source tools, and agentic AI to develop reliable, technology-aware circuit-design workflows.

Mehdi Saligane is an Assistant Professor of Engineering at Brown University and a Visiting Faculty Researcher at Google Research. His research focuses on AI-assisted chip design, analog and mixed-signal design automation, and energy-efficient hardware for AI. He is a founding member of the OpenROAD project and Chair of the IEEE SSCS Technical Committee on Open-Source Ecosystems. He also served as Chair of the CHIPS Alliance Analog Working Group. He has helped lead several community initiatives, including the IEEE SSCS Chipathon and Code-a-Chip programs, that broaden access to practical integrated-circuit design and fabrication.

12:00 – 12:15 PM Adjourn and feedback

BCICTS 2026 PRIMER
ESSEX CENTER

Time: 1:00 PM – 5:00 PM
Topic: Millimeter-wave Design, Packaging, and Measurements

Speakers:

- Dr. Akshar Visweswaran, Nokia Bell Labs
- Prof. Madhavan Swaminathan, Penn State University
- Dr. Luciano Boglione, Boeing

12:15 – 1:00 PM **Lunch**
Essex North

1:00 – 1:10 PM **Welcome**
Leo Vera, Celero Communications

1:10 – 2:10 PM **Millimeter Wave FMCW Radar Systems**
Instructor: Dr. Akshay Visweswaran, Nokia Bell Labs

Abstract: Millimeter-wave FMCW radars offer a compelling combination of a compact form factor, wide bandwidth, and high spatial resolution. This talk covers the fundamentals of FMCW radar operation and delivers insight on system-level trade-offs in broadband radar architectures, with particular emphasis on MIMO techniques for improved spatial sensing. The interplay between waveform parameters, available bandwidth, antenna configuration, and transceiver performance is discussed from a system perspective. Aspects of transceiver design, signal processing considerations, and examples of integrated millimeter-wave FMCW radar systems complete the outline of modern FMCW radar systems.

Akshay Visweswaran received the M.Sc. and Ph.D. degrees in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2009 and 2017, respectively. He was an Analog/RF Designer with Conexant Systems, Hyderabad, India, from 2006 to 2007, and the IC-Laboratory, NXP, Eindhoven, The Netherlands, from 2009 to 2010. He joined imec, Leuven, Belgium, in 2015, as a Senior Researcher, where he was the Technical Project Lead for radar and communication programs beyond 100 GHz from 2017 to 2021. From 2021 to 2022, he was a Principal RF Engineer with the Huawei Technologies R&D Center, Leuven. He is currently a Senior Research Scientist with Nokia Bell Labs, Murray Hill, NJ, USA. His interests include system modeling and the design and characterization of integrated systems for wireless and wireline applications. Dr. Visweswaran serves as a Technical Program Committee Member at ISSCC, ESSERC, BCICTS and EuMW. He was a recipient of the Top-Talent Fellowship during his M.Sc. study at TU Delft. While at imec, he led the RFIC design leg of the EU Horizon-2020 Project, Taranto, which won the Best Technology Pioneer Award at European Forum for Electronic Components and Systems (EFECS) 2020. He serves as a reviewer for several IEEE journals.

2:10 – 2:25 PM **Coffee Break**

2:25 – 3:25 PM **Advanced Packaging for mmWave Systems**
Instructor: Prof. Madhavan Swaminathan, Penn State University

Abstract: Wireless communication requires supporting large bandwidth, which can be enabled through frequencies in the

sub-Terahertz frequency range. This requires integration of high frequency composite materials and III-V semiconductor integrated circuits (IC) into a heterogeneous stack using embedded dies and 3D vertical interconnections. Advanced packaging becomes extremely critical in such applications.
This tutorial will start with the basics, cover existing and emerging materials that can be used for integration supported by process recipes and integration results. Some of the lowest loss interconnect structures based on a vertical integration concept will be discussed along with its comparison with state of the art.

Madhavan Swaminathan is the Department Head of Electrical Engineering and is the William E. Leonhard Endowed Chair at Penn State University. He also serves as the Director for the Center for Heterogeneous Integration of Micro Electronic Systems (CHIMES), an SRC JUMP 2.0 Center. Prior to joining Penn State, he was the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE), Professor in ECE with a joint appointment in the School of Materials Science and Engineering (MSE), and Director of the 3D Systems Packaging Research Center (PRC) – a graduated NSF-Engineering Research Center (ERC), Georgia Tech (GT). Prior to GT, he was with IBM working on packaging for supercomputers. Prof. Swaminathan's interdisciplinary research on semiconductor packaging and systems integration over the years have resulted in 650+ technical publications, 200+ invited presentations (seminars, keynotes, panels), 3 books, 5 book chapters, 31 patents, 35 best paper and student paper awards, 5 GT awards, 2 start-ups, and several international recognitions with the recent one being the 2024 IEEE Rao R. Tummala Electronics Packaging Award (highest technical field award in packaging) for "contributions to semiconductor packaging and system integration technologies that improve the performance, efficiency, and capabilities of electronic systems". He is also the founder of the IEEE Conference on Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the IEEE Electronics Packaging Society (EPS). He is a Fellow of IEEE, Fellow of the National Academy of Inventors (NAI), Fellow of Asia-Pacific Artificial Intelligence Association (AAIA), and has served as the Distinguished Lecturer for the IEEE Electromagnetic Compatibility (EMC) society. He serves as an advisor to India Semiconductor Mission and on the external advisory board for Move2THz (an EU initiative), as well as advisor to 3DGS and Claros. He received his MS and PhD degrees in Electrical Engineering from Syracuse University, USA.

3:25 – 3:40 PM Coffee Break

3:40 – 4:40 PM Measuring Noise Parameter: An Alternative, Size-Based Approach for On-Wafer Device Characterization
Instructor: Dr. Luciano Boglione, Boeing

Abstract: This talk will discuss and demonstrate a recent technique developed to characterize the noise parameters of microwave active devices. This innovative approach makes use of the device size as the tuning element to measure the device noise figure from which the noise parameters are extracted. This method provides an effective solution to remove the main bottleneck that makes the measurement of the noise parameters both tedious and burdensome: the requirement of an input tuner. When measuring the noise figure of a set of similar devices with different sizes, the input tuner is no longer required. Modern network analyzers are employed in lieu of noise figure meters offering a fast solution to determining the device's noise parameters without the additional overhead of characterizing the tuner itself. The clear advantage of this solution is that noise parameters can be

measured over a wide frequency, bias and temperature range. Measurement automation can be easily implemented as well. The presentation will describe this technique in detail, present measurement data and explain how it can be applied to characterize any two-port active devices.

Luciano Boglione was born in Turin, Italy, where he received his Laurea degree in Electronic Engineering from the Politecnico di Torino, Italy. He received his PhD from the Institute of Microwaves, School of Electrical and Electronic Engineering, the University of Leeds, UK, under the supervision of the late Prof. Roger Pollard. He has 25+ years of experience in the design and characterization of monolithic microwave and radio frequency integrated circuits (RFICs) fabricated in advanced technologies. His professional experience embraces industry, academia, and government institutions. In 2011, he joined the U.S. Naval Research Laboratory, Washington, DC, USA, where he has led efforts to design advanced subsystems in silicon technology for full-duplex applications. In addition, he continued to develop his long-time interests related to new microwave noise characterization techniques in support of integrated designs. In 2024, Dr. Boglione joined the Boeing Company where he has been involved in new programs and projects spanning cryogenic noise characterization and photonic designs. Dr. Boglione has published more than 45 articles in peer-reviewed publications and holds three patents. He is also a reviewer of several peer-reviewed publications and conferences. Dr. Boglione was an elected AdCom Member of the MTT Society for two terms (2007-2012). He is also a member and a past Chair of the MTT-S Microwave Low-Noise Techniques Committee. He was the 2007 RFIC Conference General Chair and the 2024 Government Microcircuit Applications & Critical Technology Conference (GOMACTech) General Chair. Dr. Boglione continues to be an IEEE Volunteer in various capacities.

4:40 – 5:00 PM Primer Wrap-Up

MONDAY

INTRODUCTORY REMARKS AND PLENARY

WELCOME AND ANNOUNCEMENTS

9:30-10:00 AM

Essex Ballroom South

Jack Pekarik, Symposium Chair

PLENARY SESSION

10:00 AM-12:00 PM

Essex Ballroom South

Session Chair: Jack Pekarik, GlobalFoundries

Co-Chair: Tomislav Suligoj, *University of Zagreb*

10:00-11:00 AM

"Vibe Design" of Analog, RF and Microwave Integrated Circuits: Future Directions

Lawrence Larson

Brown University

11:00 AM-12:00 PM

AlScN/GaN RF HEMTs: From Single to Multiple Channels

Debdeep Jena

Cornell University

CONFERENCE PROGRAM

1a. Compound Advanced Devices and Technology

Monday 1:30 PM ***Essex North & Center***

Session Chair: Junji Kotani, *Sumitomo Electric*

Co-Chair: Bruce Green, *NXP*

1a.1 (Invited)

1:30-2:10 PM – High Power, Low Thermal Resistance, X-band GaN HEMTs

David Brown[1], Puneet Srivastava[1], Bill Zivasatienraj[1], Louis Mt. Pleasant[1], Anthony Romano[1], Kanin Chu[1], Isaac Wildeson[1], Craig McGray[2], Sean O'Leary[2], Robert Henry[2], Srabanti Chowdhury[3], Kelly Woo[3], Mohamadali Malakoutian[3], Sukwon Choi[4], Seokjun Kim[4], Daniel C. Shoemaker[4], Husam Walwil[4], Kyeongjae Cho[5], Youhwan Jo[5], Yu-Eng Jeng[6], Patrick Fay[6]

[1] Electronic Systems, BAE Systems Inc.

[2] Modern Microsystems Inc.

[3] Department of Electrical Engineering, Stanford University

[4] Department of Materials Science and Engineering, Pennsylvania State University

[5] Material Science Engineering, University of Texas at Dallas

[6] Department of Electrical Engineering, University of Notre Dame

1a.2

2:10-2:30 PM – Optimization of Multi-Contact 3-Dimensional AlGaN/GaN SLCFET Diodes with High Work Function Metal for Improved Rectifying Behavior and Reliability

Annaliese Drechsler, Hannah Masten, Brian Alt, Justin Parke, Joseph Lee

Advanced Technology Laboratory, Northrop Grumman Mission Systems

1a.3
2:30-2:50 PM – Multi-Finger Transferred-Substrate InP/GaAsSb DHBTs-on-Si for D-Band Power Amplifiers
Andrea Cercaci, Filippo Ciabattini, Sara Hamzeloui, Mojtaba Ebrahimi, Olivier Ostinelli, Colombo R. Bolognesi
Millimeter-Wave Electronics (MWE) Group, ETH Zurich

1a.4
2:50-3:10 PM – 0.2 µm-Wide-Emitter InP/InGaAs DHBTs With a 30-nm-Wide InGaAsP/InP Composite Ledge Exhibiting fmax>800 GHz and High β ~ 45
Yuta Shiratori, Yusuke Araki, Takuya Hoshi, Shiro Ozaki, Shuhei Arai, Fumito Nakajima
Device Technology Labs, NTT, Inc., Japan

1b. Next-gen BiCMOS and AI for Inverse Design

Monday 1:30 PM ***Essex South***
Session Chair: Alexander Fox, IHP
Co-Chair: Kai Kwok, Skyworks

1b.1 (Invited)
1:30-2:10 PM – Enabling High-Speed Communication with Next-Generation SiGe HBTs
Arvind Narayanan[1], Uppili Raghunathan[2], Steven Shank[2], and Vibhor Jain[3]
[1]GlobalFoundries, Austin, TX
[2]GlobalFoundries, Essex Junction, VT
[3]GlobalFoundries, Malta, NY

1b.2
2:10-2:30 PM – Complementary f_T Doublers in a High Performance SiGe CBiCMOS Process
Uppili Raghunathan[1], Steven Shank[1], Sarah McTaggart[1], Megan Lydon-Nuhfer[1], Aaron Vallett[1], Saurabh Sirohi[1], Vibhor Jain[2], and John J. Pekarik[1]
[1]GlobalFoundries, Essex Junction, VT
[2]GlobalFoundries, Malta, NY

1b.3 (Invited)
2:30-3:10 PM – AI and TCAD for Inverse Design and Defect Discovery: From Machine Learning to LLM
Hiu Yung Wong
San Jose State University

Panel Sessions

Monday 3:40 PM ***Essex South***

3:40-4:40 PM – WIE/YP Panel: AI in Engineering Design: Opportunities, Challenges, and the Road Ahead

4:45-5:45 PM – The GaN-on-Si Revolution: Hype or Reality?

TUESDAY

2a. Designing with GaN: LNAs, PAs, and Beyond

Tuesday 8:30 AM ***Essex North & Center***
Session Chair: Simon Mahon, *Macquarie University*
Co-Chair: Mauricio Pinto, *Qorvo*

2a.1
8:30-8:50 AM – Design of a robust X-band LNA using a 0.12 µm GaN Technology
Leo B. Y. Poon, David J. Niven, Evan S. Shelley, Melissa C. Gorman, Anthony E. Parker, and Simon J. Mahon
School of Engineering, Macquarie University, Australia

2a.2
8:50-9:10 AM – 32–38 GHz GaN MMIC Traveling-Wave Power Amplifier
John Bucceri and Michael Litchfield
BAE Systems - ES Microelectronics

2a.3
9:10-9:30 AM – A 13-17 GHz Dynamic Power Splitter for Gain Improvement of Multi-branch Power Amplifiers
Dimos Tikeris[1], Hossein Zaheri[1], Rickard Stahl[2], Baktash Behmanesh[3], Christian Fager[1], and Gregor Lasser[1]
[1]*Microwave Electronics Laboratory, Chalmers University of Technology, Sweden*
[2]*Saab, Sweden*
[3]*Department of Electrical and Information Technology, Lund University, Sweden*

2a.4
9:30-9:50 AM – A Two-stage, 30-GHz GaN Power Amplifier with CMOS SOI Adaptive Biasing Circuitry for 1-dB Compression Improvement
Justin J. Kim, Nicholas Vong, Bennett C. Coy, Janani Ganesh, Lukas Kielbasinski, Mark R. Soler, Florian Herrault, and James F. Buckwalter
PseudolithIC, USA

2a.5
9:50-10:10 AM – 80 W S-Band Power Amplifier with Stitched FET Layout in 0.12 µm GaN
David J. Niven, Andrew J. Jones, Evan S. Shelley, Melissa C. Gorman, and Simon J. Mahon
School of Engineering, Macquarie University, Australia

2b. High-Performance Circuits for Optical Communications

Tuesday 8:30 AM ***Essex South***
Session Chair: Munehiko Nagatani, NTT Inc.
Co-Chair: Bryan Bruins, fJscaler Inc.

2b.1 (Invited)
8:30-9:10 AM – High-Speed Electronics for AI Scaling
Xin Yin, Leandro da Silva, Nishant Singh, Jakob Declercq, Shengpu Niu, Cheng Wang, Gertjan Coudyzer, Bart Moeneclaey, Guy Torfs, Peter Ossieur, Johan Bauwelinck
IDLab, imec – Ghent University

2b.2
9:10-9:30 AM – 128-GBaud Complementary HBT Inverter TIA in 130-nm SiGe BiCMOS Technology
Sarah Bahnam[1], Peter Schvan[2], and Sorin P. Voinigescu[1]
[1]*University of Toronto, Toronto, ON, Canada*
[2]*Ciena Canada Corp., Ottawa, ON, Canada*

2b.3
9:30-9:50 AM – A 50-GHz Fully-Differential SiGe BiCMOS Transimpedance Amplifier for 100-GBd Optical Receivers
Jakob Declercq, Shengpu Niu, Cheng Wang, Joris Lambrecht, Bart Moeneclaey, Xin Yin
IDLab, Department of Information Technology, Ghent University

3a. Modeling of Polarization and Memory Effects in GaN

Tuesday 10:40 AM ***Essex North & Center***
Session Chair: Ujwal Radhakrishna, Texas Instruments
Co-Chair: Rob Jones, BAE Systems

3a.1 (Invited)
10:40-11:20 AM – Characterization of Low-Frequency Memory Effects in GaN HEMTs with a New Real-Time NVNA
Patrick Roblin, Miles Lindquist, Matthew J. Nichols, and Dominic Mikrut
Dept. of Electrical and Computer Engineering, The Ohio State University, United States

3a.2
11:20-11:40 AM – What Are Non-Arrhenius Trapping Effects in GaN HEMTs
Carter Mayfield and Nicholas C. Miller
Dept. of Electrical and Computer Engineering, Michigan State University, United States

3a.3
11:40 AM-12:00 PM – Revising the Polarization Model in AlGaN/(AlN)/GaN HEMTs with M-Polar and N-Polar Barriers
Mario Marušić, Dario Novaković, Ivan Berdalović, and Tomislav Suligoj
Faculty of Electrical and Computing, University of Zagreb, Croatia

3b. Transmitter Circuits for Optical Communications

Tuesday 10:40 AM ***Essex South***
Session Chair: Bryan Bruins, fJscaler Inc.
Co-Chair: Romain Hersent, Nokia Bell Labs

3b.1
10:40-11:00 AM – 180-GHz and 235-GHz Bandwidth DC-Coupled Cascaded Distributed Amplifiers in 250-nm and 200-nm InP DHBT Technology
Teruo Jyo, Munehiko Nagatani, Yuta Shiratori, Yusuke Araki, Hiroyuki Takahashi
Device Technology Labs, NTT, Inc.

3b.2
11:00-11:20 AM – A 160-GBd PAM-4 Linear Distributed Modulator Driver with 167 GHz Bandwidth in 130-nm SiGe BiCMOS
Robert Huber[1], Thiemo Herbel[1], Anna Peczek[2], Lars Zimmermann[3], Dietmar Kissinger[1]
[1]Institute of Electronic Devices and Circuits, Ulm University, Germany
[2]IHP – Leibniz Institute for High Performance Microelectronics, Germany
[3]FG Silizium-Photonik, Technische Universität Berlin, Germany

3b.3
11:20-11:40 AM – A 357-GS/s InP/GaAsSb DHBT 2:1 Analog Multiplexer
T. Jian[1], S. Hamzeloui[2], J. Zhao[1], S. Pati Tripathi[1], O. Ostinelli[2], C. R. Bolognesi[2], P. Schvan[3], and S. P. Voinigescu[1]
[1]University of Toronto, Toronto, ON, Canada
[2]ETH Zurich, Zurich, Switzerland
[3]Ciena Canada Corp., Ottawa, ON, Canada

4a. mmW Receiver and Transmitter Technologies

Tuesday 1:30 PM ***Essex North & Center***
Session Chair: Najme Ebrahimi, *Northeastern University*
Co-Chair: Kevin Kobayashi, *Qorvo*

4a.1 (Invited)
1:30-2:10 PM – Receiver and Transmitter Multifunction MMICs in InP DHBT and SiGe BiCMOS Technologies for High Datarate Communication and Sensor Systems above 100 GHz
Herbert Zirath, Vessen Vassilev, Yu Yan, and Frida Strömbeck
Chalmers University, Gothenburg, Sweden

4a.2
2:10-2:30 PM – A 61–98-GHz Wideband Receive Beamformer with 4.7–6.8 dB NF for E/W-Band Applications in 90-nm SiGe BiCMOS Process
Ahmed Helaly, Mohammed Helal, Gabriel M. Rebeiz
University of California, San Diego, USA

4a.3
2:30-2:50 PM – A 57-96 GHz Wideband Transmit Beamformer for Multi-Band Phased-Array Systems in 90-nm SiGe BiCMOS
Mohammed Helal, Ahmed Helaly, Gabriel M. Rebeiz
University of California, San Diego, USA

4a.4
2:50-3:10 PM – A Noise-Matched 8 mW D-band LNA with 14.6 dB Gain and 7.5 dB NF in BiCMOS Technology
Pierre-Louis Hellier*†, Hervé Barthélemy†, Sylvie Lepilliet‡, Yewulsew Manale Wodaje‡, Pascal Szriftgiser§, Guillaume Ducournau‡, Florence Podevin*, and Sylvain Bourdel*
* *TIMA UMR CNRS 5159, Univ. Grenoble Alpes, Grenoble, France*
† *IM2NP UMR CNRS 7334, Univ. Toulon, Toulon, France*
‡ *IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille, Univ. Polytechnique Hauts-de-France, Villeneuve d'Ascq, France*
§ *PhLAM UMR CNRS 8523, Univ. Lille, Lille, France*

4a.5
3:10-3:30 PM – An Ultra Low-Power Compact D-band LNA in 22-nm FDSOI CMOS for Massive-Scale Phased-Array Systems
Kwangwon Park, Yuya Nemoto, Alex Dinkelacker, Mark Rodwell
Department of Electrical and Computer Engineering, University of California Santa Barbara, CA USA

4b. Advances in Compact & Analytical Modeling; RF & mm-wave Measurement Tools and Techniques

Tuesday 1:30 PM ***Essex South***
Session Chairs: Nicolas Derrier, *STMicroelectronics*, Sirohi Saurabh, *Global Foundries*
Co-Chairs: Peter Zampardi, *Qorvo*, Sadayuki Yoshitomi, *Megachips Corp.*

4b.1 (Invited)
1:30-2:10 PM – Key Challenges of SPICE-Based Compact Modeling for Silicon Photonics
Abdelsalam Aboketaf, *Global Foundries*

4b.2
2:10-2:30 PM – Investigation of vertical non-quasi-static effects in SiGe HBTs using a new approach for large-signal compact model development
Mario Krattenmacher[1,2] and Michael Schröter[1,3]
[1]*Chair for Electron Devices and Integrated Circuits, TU Dresden, Dresden Germany*
[2]*SemiMod GmbH, Germany*
[3]*ADM Enterprises, Escondido, USA*

4b.3 (Invited)
2:30-3:10 PM – Measurement Progress That Moves the BCICTS Community Forward
Andrej Rumiantsev[1], Jiapin Guo[2], Bryan Hosein[2], and Vincent Gillet[3]
[1]MPI Corporation
[2]Focus Microwaves
[3]Keysight Technologies

4b.4
3:10-3:30 PM – A compact bias and current dependent model for the electric field in the collector of high-breakdown HBTs
Michael Schröter[1,3] and Mario Krattenmacher[1,2]
[1]Chair for Electron Devices and Integrated Circuits, TU Dresden, Dresden Germany
[2]SemiMod GmbH, Germany
[3]ADM Enterprises, Escondido, USA

5a. Ultra High Frequency Circuit and System Design Techniques

Tuesday 4:00 PM ***Essex North & Center***
Session Chair: Damla Dimlioglu, *Cornell University*
Co-Chair: Kazuya Yamamoto, *Mitsubishi Electric Corporation*

5a.1 (Invited)
4:00-4:40 PM – Closing the RFIC Design Productivity Gap Through AI-Assisted RFIC Design Automation
Sensen Li[1], Taiyun Chi[2], David Z. Pan[1]
[1]The University of Texas at Austin, Austin, TX, USA
[2]Rice University, Houston, TX, USA

5a.2 (Student)
4:40-5:00 PM – A Wideband mm-Wave PLL with High Output Power and Efficiency in 90-nm SiGe BiCMOS
Benyamin Fallahi Motlagh, Aydin Babakhani
University of California, Los Angeles, CA, USA

5a.3 (Student)
5:00-5:20 PM – A 500–600–GHz Transmitter for Gas Spectroscopy in a 130–nm BiCMOS Technology
Marco Hippich[1], Leon Spießhofer[1], Lars Zimmermann[2], Dietmar Kissinger[1]
[1]Institute of Electronic Devices and Circuits, Ulm University, Germany
[2]Leibniz Institute for High Performance Microelectronics, Frankfurt (Oder), Germany

5a.4 (Invited)
5:20-6:00 PM – Structured Compactification for RF Integration
Minoru Fujishima
Hiroshima University, Higashi-Hiroshima, Japan

5b. Analog ICs

Tuesday 4:00 PM ***Essex South***
Session Chair: Sri Navaneeth Easwaran, Texas Instruments
Co-Chair: Brian Ma, UT Dallas

5b.1 (Invited)
4:00-4:40 PM – Reliability-Aware Integrated SiC Gate Driver with Online Sequential EMI and Aging Control (Invited Paper)
D. Brian Ma, Yuanqin Huang
Integrated Power Electronics System Laboratory
Department of Electrical and Computer Engineering
The University of Texas at Dallas

5b.2
4:40-5:00 PM – Cryogenic Capless Low-Dropout Regulator in 55 nm BCD Toward PMU Integration in Shuttling Controller SoC for Ion-Trap Quantum Computer
Zhaoqun Guo, Adilet Dossanov, Y Quynh Nguyen, Yigit Kecik, Vadim Issakov
Institute for CMOS Design, TU Braunschweig, Braunschweig, Germany

5b.3
5:00-5:20 PM – On-Chip BJT-Equalized Bandgap Reference for Optically-Driven SiC Gate Drivers
Fei Zhou and D. Brian Ma
Integrated Power Electronics System Laboratory
Department of Electrical and Computer Engineering
The University of Texas at Dallas

5b.4
5:20-5:40 PM – A Compact Programmable 97 Vpp Driver for Piezoelectric Micropumps in 180 nm CMOS
Mathis Vondeberg[1], Laurenz Nilges[1], Christian Ziegler[1], Paul Shine-Eugine[1], Tim Rambousky[2], Bernhard Wicht[2], Vadim Issakov[1], Liubov Bakhchova[1]
[1]Technische Universität Braunschweig, Germany
[2]Leibniz Universität Hannover, Germany

5b.5
5:40-6:00 PM – A CMOS Active-Inductor Stochastic Processing Unit for Probabilistic AI
Mahathi Krishna Ravi Shankar, Jeff Zhang, Kexin Li
ECEE, Arizona State University, Tempe

WEDNESDAY

6a. SiGe, GaAs, InP, GaN, and Cryogenic Circuits: An Evolutionary Perspective

Wednesday 8:30 AM ***Essex North & Center***
Session Chair: Greg Flewelling, *BAE Systems*
Co-Chair: Thomas Landon, *Texas Instruments*

6a.1 (Invited)
8:30-9:10 AM – Darlington's Evolution – Survival of a fit RF Amplifier
Kevin W. Kobayashi
Qorvo – HPA Systems, Technology, and Research

6a.2
9:10-9:30 AM – A 0.74-mW Ku-band Cryogenic SiGe LNA in 130-nm BiCMOS with 14-K Noise Temperature for Scalable Quantum Readout
Xiuhan Chen[1], Haoling Li[1], Gun Suer[1], Leonardo Ranzani[2], Kin Chung Fong[1], Aravind Nagulu[1], and Najme Ebrahimi[1]
[1]Northeastern University, Boston, MA, USA
[2]RTX BBN Technologies, Cambridge, MA, USA

6a.3
9:30-9:50 AM – A New Method of Stability Margin Analysis for Designing Cryogenic SiGe RF Circuits
Jackson P. Moody, Brett L. Ringel, and John D. Cressler
School of Electrical and Computer Engineering, Georgia Tech

6a.4
9:50-10:10 AM – A Wideband 1–6 GHz LNA With High Linearity: Active-Bias Linearization and Balun-Limited OIP2
Ahmed Tulan, Mohamed Elgamal, Mohamed Weheiba, Mohamed Mobarak, and Mohamed A. Y. Abdalla
Analog Devices, Egypt

6b. Next Generation High-Frequency Device Modeling

Wednesday 8:30 AM ***Essex South***
Session Chair: Markus Müller, Rohde & Schwarz
Co-Chair: Jay Barrett, MACOM

6b.1 (Invited)
8:30-9:10 AM – CryoGaN: Towards Predictive Physics-Based Compact Models for GaN HEMTs across Bias, Geometry, and Temperature
Ruilin Wang[1], Naveen Chander Prabakaran[1], Siddhant Gangwal[1], Katerina Raleva[2], Dragica Vasileska[1], and Kexin Li[1]
[1]ECEE, Arizona State University, United States
[2]EEIT, Ss. Cyril and Methodius University of Skopje, North Macedonia

6b.2
9:10-9:30 AM – Investigation of Millimeter-Wave GaN HEMT Modeling for E-Band Power Amplifier Design
Dashiel Matlock, Dave Frey, Edward Gebara, and Nicholas C. Miller
Dept. of Electrical and Computer Engineering, Michigan State University, United States

6b.3
9:30-9:50 AM – Physics-Informed Neural Network Framework for Predicting Device Electrostatics and Characteristics in Gallium Oxide MOSFETs
Tasnia Jahan and Kexin Li
Arizona State University, United States

7a. mm-Wave III-V IC Measurements and Power Generation

Wednesday 10:40 AM ***Essex North & Center***
Session Chair: Amir Alizadeh, *Keysight Technologies*
Co-Chair: Sunil Rao, *HRL Laboratories*

7a.1 (Invited)
10:40-11:20 AM – mm-Wave Measurements of GaN HEMTs: Systems, Verification Techniques, and Challenges
N. C. Miller, D. Matlock, and T. Bonnen
Michigan State University, USA

7a.2
11:20-11:40 AM – A Broadband Watt-level *E*-Band MMIC PA in 90-nm GaN HEMT Technology
S. Chen, V. Kumar, J. Zhang, and Y. Cao
Qorvo Inc. USA

7a.3 (Student)
11:40 AM-12:00 PM – InP HEMT Load-Pull Performance Demonstrating 46% PAE at *D*-Band Frequencies
J. A. Molles[1,4], J. Cheron[1,5], R. D. Jones[1,3], W. Deal[2], X. Mei[2], B. Jamroz[1], C. Evanovich[1,3], P. Aaen[3], and B. T. Bosworth[1,4]

[1] National Institute of Standards and Technology, CO, USA
[2] Northrop Grumman Corporation, CA, USA
[3] Colorado School of Mines, CO, USA
[4] Southeastern University Research Association, USA
[5] University of Colorado Boulder, Boulder, CO, USA

7a.4
12:00-12:20 PM – A 32.7-dBm High-Gain *W*-Band GaN PA MMIC Using a Reliability-Verified 0.1-µm GaN HEMT Technology
K. Hsu[1,2], J. Chung[1], C. Lin[2], K. Lin[2], J. Lin[1], S. Cheng[1], K. Chen[1], C. Chan[1], K. Matsushita[1], Y. Lin[1], and C. Lin[1,3]
[1]WIN Semiconductors, Taiwan
[2]National Taiwan University, Taiwan
[3]Lunghua University of Science and Technology, Taiwan

7b. High Performance SiGe BiCMOS and Electrostatic Doped Devices

Wednesday 10:40 AM ***Essex South***
Session Chair: Hiroshi Yasuda, Texas Instruments
Co-Chair: Tomislav Suligoj, University of Zagreb

7b.1 (Invited)
10:40-11:20 AM – Advances in SiGe-BiCMOS Technology for High-Data-Rate Communication Systems
Holger Rucker
IHP – Leibniz Institute for High Performance Microelectronics

7b.2
11:20-11:40 AM – Cryogenic characterization of SiGe HBTs
Asif Ali Mir, Christian Wipf, Gerhard Kahmen, and Holger Rucker
IHP – Leibniz Institute for High Performance Microelectronics

7b.3 (Invited)
11:40 AM-12:20 PM – More (than Moore) Electrostatic Doping
Raymond J.E. Hueting
University of Twente

8a. Late News 1

Wednesday 1:50 AM ***Essex North & Center***
Session Chair: Guanghai Ding, *Analog Devices, Inc.*
Co-Chair: Simon Mahon, *Macquarie University*

8a.1
1:50-2:10 PM – RF Performance of GaN High Electron Mobility Transistors in 200-mm GaN-on-Si Production Technology for FR1 and FR3 Applications
A. Raman, J. Arora, A. Bharadwaj, R. Wolf, Y. Ngu, R. Rassel, T. Ethirajan, I. McCallum-Cook, P. Justison, K. Parr, R. Mahmood, C. Christiansen, J. Costa, and D. Denninghoff
GlobalFoundries, Essex Junction, USA

8a.2
2:10-2:30 PM – A Heterogeneously-Integrated, Ka-band GaN LNA with 23.5 dB Gain and 2.2 dB Noise Figure
A. Dinkelacker, J. J. Kim, B. C. Coy, L. Kielbasinski, J. Ganesh, S. Scodellaro, B. Werner, F. Herrault, and J. F. Buckwalter
PseudolithIC, Inc. USA

8a.3
2:30-2:50 PM – Compact Differential Input, Single-Ended Output, X-band GaAs LNA
S. J. Mahon, D. J. Niven, A. J. Jones, E. S. Shelley, and M. C. Gorman
Macquarie University, NSW, Australia

8a.4
2:50-3:10 PM – J-Band Characterization of the Noise Parameters of InP/GaAsSb DHBTs from Measured Y-Parameters
S. P. Tripathi[1], S. Hamzeloui[2], O. Ostinelli[2], C. R. Bolognesi[2], and S. P. Voinigescu[1]
[1] University of Toronto, Toronto, Canada
[2] ETH Zurich, Zurich, Switzerland

8a.5
3:10-3:30 PM – A High Voltage Normally-Off Recessed p-NiO Gate Reverse-Conducting GaN HEMT Monolithically Integrated with Anti-Parallel GaN SBD
Lei Xie[1], Tao Zhang[1], Shengrui Xu[1], Huake Su[1], Xiangdong Li[2], Xu Liu[1], Yue Hao[1], and Jincheng Zhang[1]
[1] State Key Laboratory of Wide-Bandgap Semiconductor Devices and Integrated Technology, School of Microelectronics, Xidian University, Xi'an, China
[2] Guangzhou Wide-Bandgap Semiconductor Innovation Center, Guangzhou Institute of Technology, Xidian University, Guangzhou, China

8b. Late News 2

Wednesday 1:50 AM ***Essex South***
Session Chair: Damla Dimlioglu, *Cornell University*
Co-Chair: Farooq Amin, *Macom*

8b.1
1:50-2:10 PM – Broadband 180-GBd PAM-4 Transimpedance Amplifiers Utilizing Lattice Filters for Group Delay Equalization in 130-nm SiGe BiCMOS
T. Herbel[1], A. Peczek[2], L. Zimmermann[2,3], and D. Kissinger[1]
[1] Institute of Electronic Devices and Circuits, Ulm University, Germany
[2] Leibniz Institut für Innovative Mikroelektronik (IHP), Germany
[3] FG Silizium-Photonik, Technische Universität Berlin, Germany

8b.2
2:10-2:30 PM – A 95–130 GHz Up-Converter with Reconfigurable High-Pass Filter and 30–55 dB Spur Rejection in 22-nm FD-SOI
Y. Zuo and G. M. Rebeiz
University of California San Diego, San Diego, USA

8b.3
2:30-2:50 PM – A 95–127 GHz Beamforming Transmitter Front-End with 12 dBm Peak P_{sat} and Low RMS Phase and Gain Errors in 22-nm FD-SOI
Y. Zou, H. Ju, and G. M. Rebeiz
University of California San Diego, San Diego, USA

8b.4
2:50-3:10 PM – A 10 GHz 1-to-3 Active Power Divider with Single-Inductor Splitting Core, >55 dB Isolation and 1.6° Phase Imbalance in 22 nm FD-SOI
D. F. Stein, J. Romstadt, R. Zhou, C. Ziegler, F. Stapelfeldt and V. Issakov
Institute for CMOS Design, TU Braunschweig, Germany

8b.5
3:10-3:30 PM – Design Optimization Methodology of a 62-GHz Pseudo-Differential LNA in 22nm-FDSOI
N. Elsayed, C. Zhang, S. Sheibani, and A. Bellaouar
GlobalFoundries, USA

LOOKING TOWARDS THE FUTURE

The 2027 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)

will be held on October 17-20, 2027

San Diego, California, USA

INTEGRATED CIRCUITS and DEVICES in GaAs, InP, GaN, SiGe, and other compound semiconductor and CMOS technologies

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CALL FOR PAPERS

The 2027 BCICTS will be held in San Diego, California, USA October 17-20, 2027. Subject area groupings for paper submissions are as follows:

HIGH-SPEED DIGITAL, MIXED-SIGNAL, AND OPTOELECTRONIC ICs, Mixed analog/digital ICs – Digital ICs – (high-speed) DACs and ADCs – Networking ICs, MUX/DEMUX, Clock and data recovery, Decision circuits, Equalizers – Optical data links, Laser and modulator drivers, optoelectronics and photonics ICs

ANALOG, RF, AND MICROWAVE ICs
Op amps – Voltage references and regulators – Integrated filters – Sensors and actuators – RF circuits and systems – Radio and transceiver subsystems – LNAs – AGCs – Mixers – Voltage controlled oscillators – Frequency synthesizers – Power amplifiers – RF switches – Noise and distortion suppression – RF Packaging – Integrated RF passives. Analog, RF, power conversion, High-voltage ICs – Biomedical electronics – Power Management ICs – Energy harvesting ICs – Motor controls – Analog subsystems within a VLSI chip – Packaging of high-performance ICs.

mm-WAVE AND THZ ICs
Millimeter – wave circuits and systems – THz circuits and systems. MM-Wave switches and amplifiers. Phased-array antenna circuits

DEVICE PHYSICS:
New device physics phenomena in Si, SiGe, SiC, GaN, MOS, and III-V HBTs and FETs – Device design issues and scaling limits – Hot electron effects and reliability physics – Transport and high field phenomena – Noise – Linearity/Distortion – Novel measurement techniques – Operation in extreme environments (low/high temperatures, radiation effects), and ESD phenomena.

MODELING AND SIMULATION
Improved silicon-based BJT and HBT models and physics-based modelling techniques – Improved III-V HBT and FET models and physics-based modelling techniques – Parameter extraction methods and test structures – High-frequency measurement, calibration and de-embedding techniques – RF and thermal simulation techniques – Modelling of passives, interconnect and packages – Statistical modelling – Device, process and circuit simulation – CAD/modelling of power devices – Packaging of power devices.

PROCESS AND DEVICE TECHNOLOGY
Device and IC manufacturing processes, testing methodologies, & reliability – Integration of III-V devices on Si – High performance devices such as GaN power conversion devices – near-THz SiGe HBTs & InP HEMTs – Novel devices such as tunnel FETs (TFETs) – carbon nanotubes, MEMS, graphene & diamond transistors. Optoelectronic and photonic devices such as optical modulators, lasers, photodetectors, and Silicon Photonics – Thermal management technologies, thermal simulation – Advanced packaging of high-power devices and ICs. Advances in processes and device structures demonstrating high speed, low power, low noise, high current, high voltage, etc. BiCMOS processes – Advanced process techniques – Si and SiC homojunction bipolar/BiCMOS devices and SiGe heterojunction bipolar/BiCMOS devices – Manufacturing solutions related to Bipolar and BiCMOS yield improvements – Fabrication of high-performance passive components, sensors, and MEMs – Process technology related to discrete and integrated bipolar/BiCMOS power devices – IGBT, RF power devices. Wide bandgap bipolar devices (e.g., SiC) and related process technology – 3D Integration – Reliability and testing for IC manufacturing

IMPORTANT DATES
Friday May 7, 2027 – Abstracts Due
Friday, July 9, 2027 – Decision E-mail Sent
Friday, September 3, 2027 – Final Manuscript Due

Authors must submit an abstract (not more than 4 pages including figures and other supporting material) of results not previously published or not already accepted by another conference. Papers will be selected on the basis of the abstract.

The abstract must concisely and clearly state:

a) The purpose of the work
b) What specific new results have been obtained
c) How it advances the state-of-the-art or the industry
d) References to prior state-of-the-art
e) Sub-committee preference:
   - Analog, RF, and Microwave ICs
   - Device Physics
   - High-Speed Digital, Mixed-Signal, & Optoelectronic ICs
   - Modeling & Simulation
   - mm-Wave and THz ICs
   - Process & Device Technology

Abstracts must include: title, author(s) name(s) and affiliation(s), corresponding authors' postal and e-mail addresses, and telephone numbers. The committee will honor the authors' committee preference but reserves the right to review the paper in other categories.

Company and governmental clearances must be obtained prior to submission of the abstract.

Accepted work may be used for publicity purposes. Portions of the abstracts may be quoted in articles publicizing the Symposium. Please note on the abstract if this is not acceptable.

Abstracts (PDF only) must be submitted electronically.

Authors will be informed of a decision by July 9, 2027. Authors of accepted papers are required to submit a 4-page camera-ready PDF by September 3, 2027 for inclusion in the Symposium Digest.

Further questions on abstract submission may be addressed to the Symposium Technical Chair:

Sadayuki Yoshitomi
Megachips Corp.
TPC Chair
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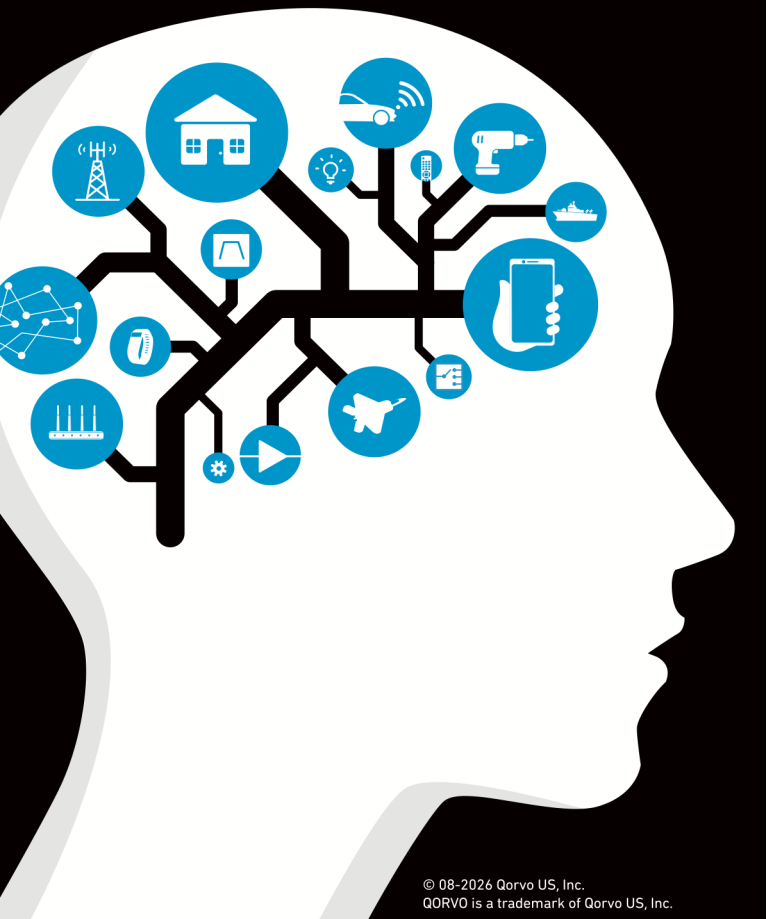

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